A 4-bit High Speed, Low Power Flash ADC by Employing Binary Search Algorithm

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Abstract

In this paper an analog to digital converter architecture is proposed. The proposed design is based on a mixed approach of flash type ADC combining with Successive Approximation Register type ADC. This new design gives lesser number of comparators compared to conventional flash ADC architecture and so, less power consumption with much low circuit complexity. For a 4-bit design it takes 7 comparators and if you go one bit higher you need two more comparators with some extra digital logic and so on. Based on this design, a 4-bit ADC is done and simulated in Cadence virtuoso Tool using 14nm CMOS technology with power supply voltage of 1.0V. The Proposed ADC consumes 242uW of power and the measured INL and DNL are 0.35 LSB and 0.38 LSB respectively.

Keywords — *Analog to Digital Converter (ADC), Comparator, Flash, DNL, INL, SFDR, SNDR.*

I. INTRODUCTION

The evolution of advanced ultra-wide band communication technologies has improved the optical communication systems and serial links. This subsequently increases the demand of high-speed and low power Analog to Digital converters having low-to-medium resolution, for converting high frequency range analog signals to digital signals for base band processing. These Ultra-wide band applications and wireless personal area networks always starve for high speed, lower resolution analog-to-digital converters [1]. Requirement of low power ADCs increasing day-by-day so that battery life can be prolonged in portable devices.

Flash ADCs are the most desired ADCs for the applications of high speed and low resolution because of their low latency and high data rate advantages. But, in Flash architecture the number of comparators in the design increases exponentially with resolution which is going to leads to increased complexity and also high power dissipation and area.

However, Successive Approximation Register (SAR) ADCs dissipates lesser power but at the cost of reduced operational speed [2].

To achieve the balance between high Speed and low power consumption, in this paper a 4-bit ADC is proposed which resembles like Flash ADC by employing Binary search algorithms. Section II describes the proposed ADC architecture. The Analysis and Simulation results for the proposed ADC and comparator are shown in section III, while conclusion is described in section IV.

II. PROPOSED ADC ARCHITECTURE BY EMPLOYING BINARY SEARCH ALGORITHM

The introduced ADC ranges in middle of flash type ADC and Successive Approximation Register type ADC category. Because of all the comparisons are carried out in single cycle and the digital code conversion is calculated using a technique similar to binary search algorithm. Below Fig. 1 shows the block diagram of proposed ADC.

In this work, five basic blocks are used (i) High speed comparator (ii) Inverter (iii) Or gate (iv) And gate and (v) Multiplexer. To meet the required specifications, these basic blocks are designed individually and then the ADC has been designed by integrating them.

The Comparator is the bottle neck of ADC which consumes the maximum power among all the other blocks. However, the proposed ADC uses 7 comparators for 4-bit ADC which is approximately half the number of comparators used by conventional flash ADC. The conventional flash ADC require 2^N-1 comparators i.e., 15, but proposed one requires comparators only at the cost of some basic digital logic gates.

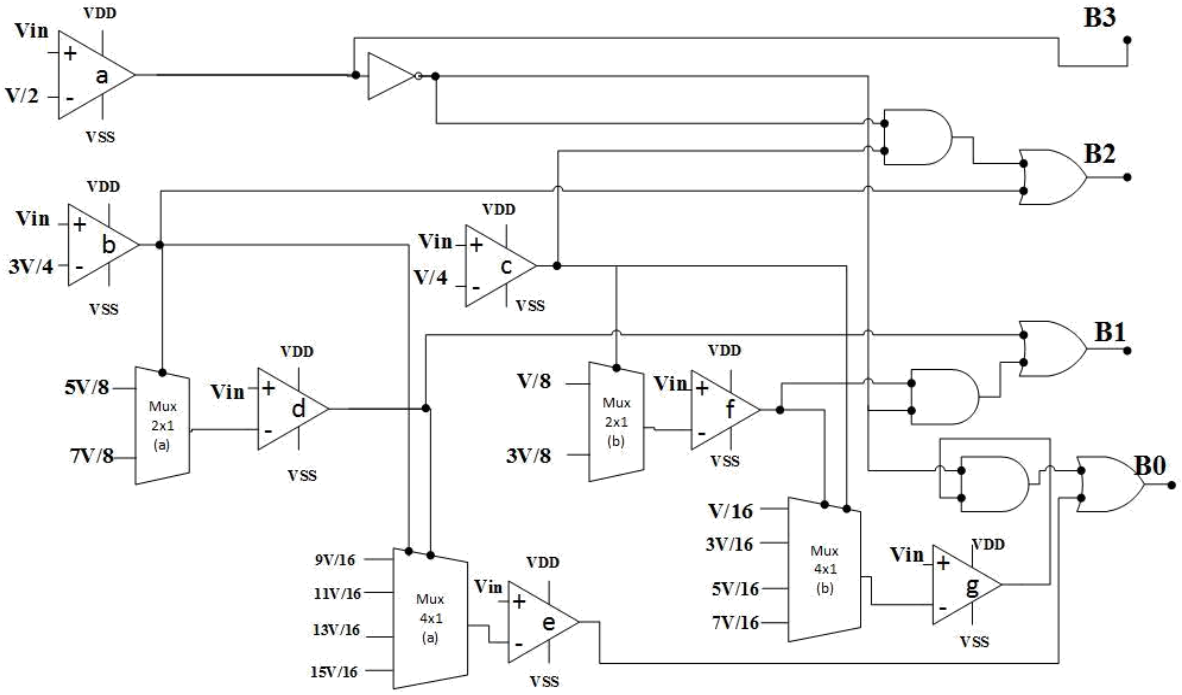

Fig. 1: Block Diagram of Proposed 4-Bit Flash ADC by Employing Binary Search Algorithm

And also if you go for 5-bit design you will be requiring two more extra comparators means only 9 comparators are required compared to conventional Flash where it requires 31.

The below Fig. 2 shows the schematic of Preamplifier based comparator. This comparator design consists of four stages, which are, input pre-amplifier, latch, self-bias differential amplifier and output buffer. The resolution of latch circuitry is very low so pre-amplifier is used to reduce the input offset voltage of the latch by the gain of pre-amplifier. The Latch circuit is also called as Decision circuit and this is the heart of the comparator and it should be capable of discriminating small mV level signals. The self-bias differential amplifier is used to amplify the latch output and buffer is used to provide enough current for the load.

Algorithm for the proposed ADC to calculate equivalent digital code corresponding to an analog voltage is given in the following steps:

1. Compare input voltage (V_{in}) with half of the reference voltage (V_{ref} =2), this gives the MSB of the equivalent digital code.
If $V_{in}>V_{(ref/2)}$ => MSB = 1, else MSB = 0;

2. To calculate MSB-1 bit:

- In case if MSB is at logic '1' then compare input
  Voltage (V_{in}) with (3/4) th of reference voltage i.e.
  (3/4)V_{ref}
- In case if MSB is at logic '0' then compare input voltage (V_{in}) with (1/4) th of reference voltage i.e.
  (1/4)V_{ref}.

To achieve this, connect MSB bit to an inverter, connect the Power supply terminal of comparator with (3/4) V_{ref} and (1/4) V_{ref}inputs to the inverter's input and output respectively.

3. Repeat steps 1 and 2 for next bits i.e. (MSB-2), (MSB- 3) and so on.

4. Use multiplexers to select comparing voltages for compara-tors depending upon previous most significant bits. A demonstration of digital code calculation by the proposed ADC is illustrated in following steps:

Step 1: Begin,
Initialize all the parameters, set values of analog input voltage
If Vin≥ V/2, set B3=High else set B3=Low

Step 2: Set inverter input = B3 then,
If B3 = High then comp (c), comp (d), comp (e) = on mode and comp (b), comp (f), comp (g) = Standby mode

And if B3 Low then comp (b), comp (f), comp (g) = on mode and comp (c), comp (d), comp (e) = Standby mode.

Step 3: If B3 = High then,
If $V_{in} \geq$ 3V/4, then set comp (c) output = High else set comp(c) Output = Low
Set B2 = output of comp (c) = output of comp (c) OR1 output of comp (b) else
If B3 =Low then,
If $V_{in} \geq$ V/4, set comp (b) output = High else set comp (b) output = Low
Set B2 = output of comp (b) = output of comp (c) OR1 output of comp (b)

Step 4: If B3 = High then
If comp (c) output is Low and $V_{in} \geq$ 5V/8, set comp (d)
output = High and
If comp (c) output is High and $V_{in} \geq$ 7V/8, set comp (d) output = High else
Set comp (d) output = Low
Set B1 = output of comp (d) = output of comp (d) OR2 output of comp (f) else
If B3 = Low then,
If comp (b) output is Low and $V_{in} \geq$ V/8, set comp (f) output =High and
If comp (b) output is High and $V_{in} \geq$ 3V/8, set comp (f) output =High else
Set comp (f) output =Low
Set B1 = output of comp (f) = output of comp (d) OR2 output of comp (f)

Step 5: If B3 =High then,
If comp (c), comp (d) output is Low and $V_{in} \geq$ 9V/16
Set comp (e) output =High and
Set B0 = output of comp (e) = output of comp (e) OR3 output of comp (g) else
If B3 =Low then,
If comp (b), comp (f) output is Low and $V_{in} \geq$ V/16, Set comp (g) output =High and
If comp (b) output is Low, comp (f) output is High and
$V_{in} \geq$ 3V/16,
Set comp (g) output = High and
If $V_{in} \geq$ 5V/16, Set comp (g) output = High and if comp (b), comp (d) output is High
And if $V_{in} \geq$ 7V/16, set comp (g) output = High else, Set comp (g) output = low
Set B0 = Output of comp (g) = Output of comp (e) OR3 Output of comp (g)
End.

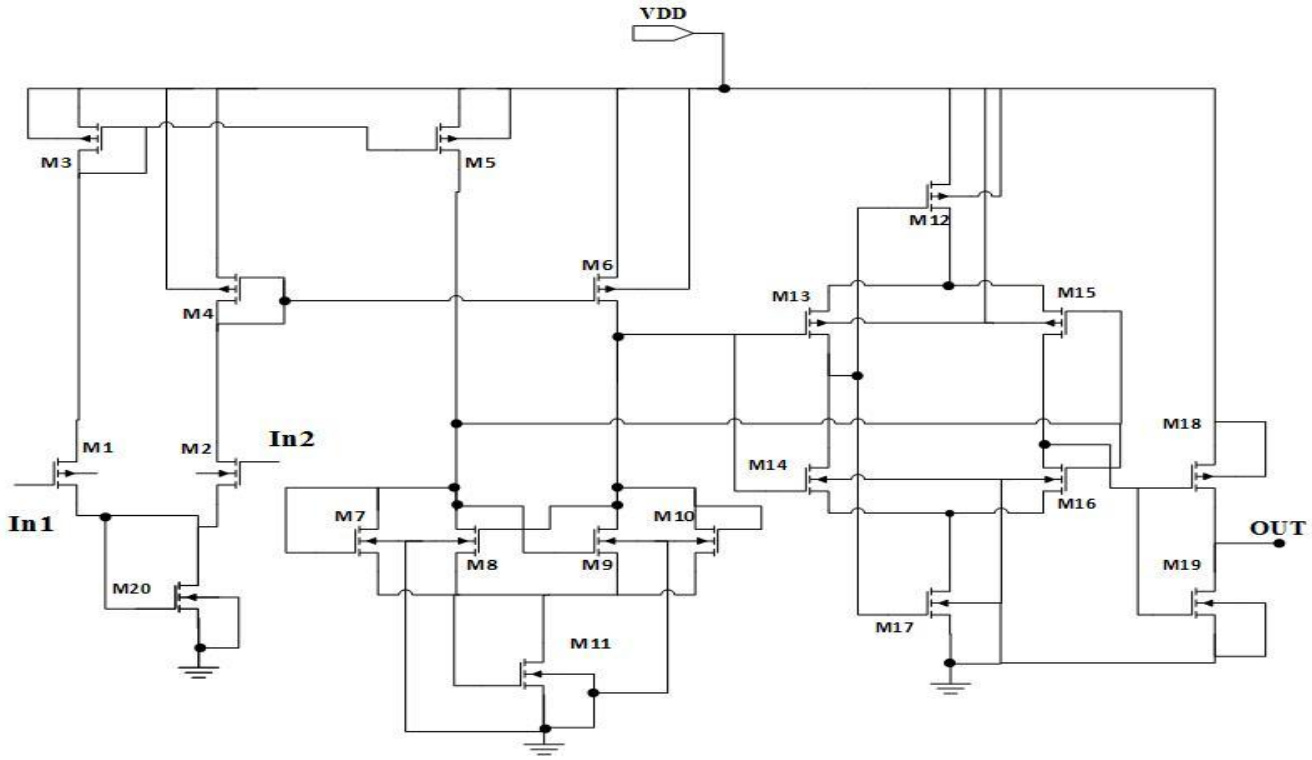

Fig. 2: Schematic Diagram of Pre-Amplifier Based Comparator

III. ANALYSIS & RESULTS

This section presents the analysis and simulation results of Comparator and proposed ADC design. The design is simulated on Cadence virtuoso with presto tool using 14nm technology file.

Fig. 3 represents the Transient analysis of Comparator. At In1, a sinusoidal input of $0.8V_{pp}$ is

applied and at In2, a DC signal of 400mV is applied. In the output you can observe a full swing square waveform in the same figure with a propagation delay of 72pSec. The measured Offset of the Comparator is 8mV and it's consuming about 34uW of power.

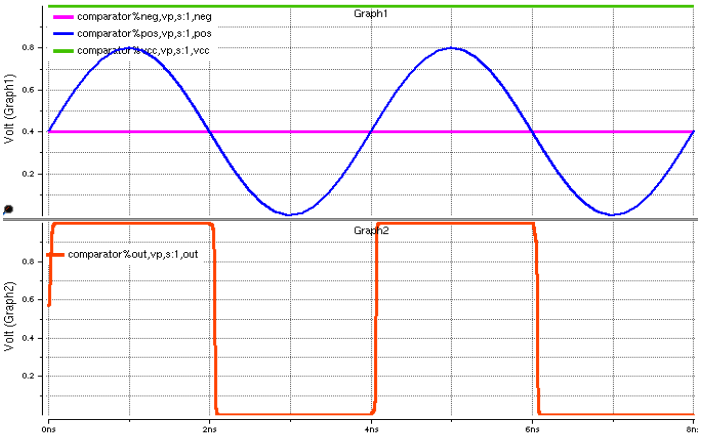

Fig. 3: Transient Analysis of Pre-Amplifier Based Comparator

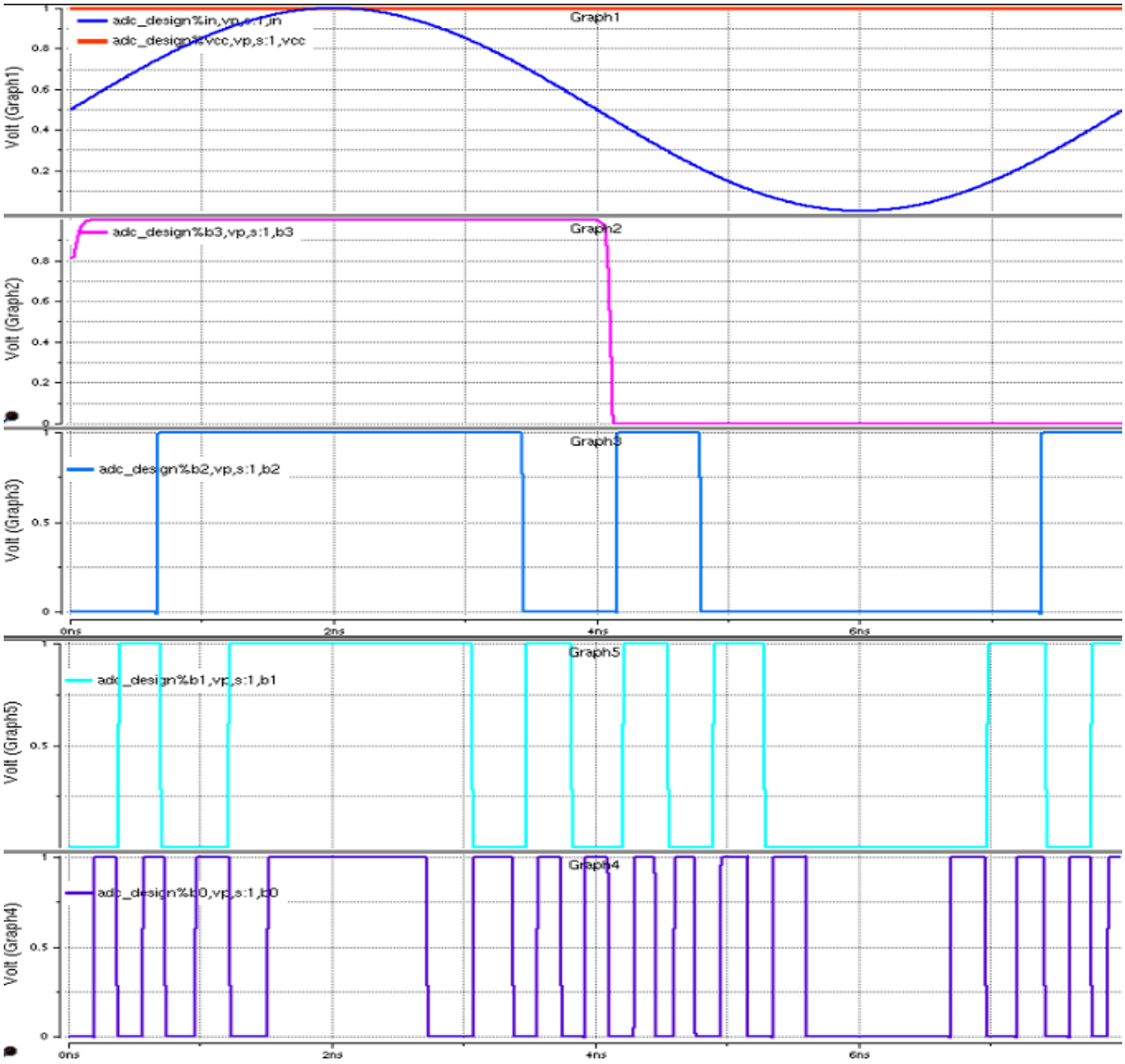

Fig. 4: Transient Analysis of 4-Bit Proposed Flash ADC With 1-Vpp Sinusoidal Input

Fig.4 shows the transient analysis of proposed ADC. At Input a Sinusoidal signal of $1V_{pp}$ is applied and simulation is done with 1V power supply. In the output you can see all the codes from 0 to 15 are coming in a full cycle of sinusoidal input, means the correct functionality of the proposed ADC.

The Static performance of the ADC can be observed from INL and DNL values obtained from the output. INL can be defined as the deviation of actual transfer function of the ADC from curve and DNL is defined as the difference step width and the ideal value of 1LSB [3].

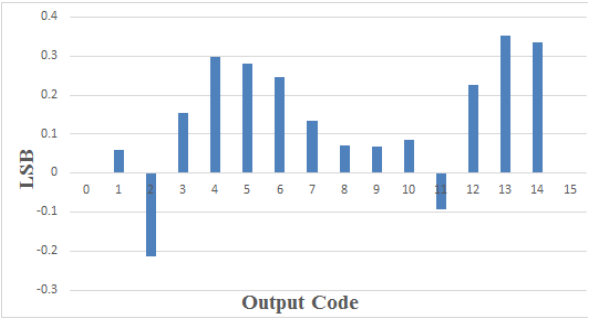

Fig.5: INL Plot of Proposed ADC from 0 To 15 Codes

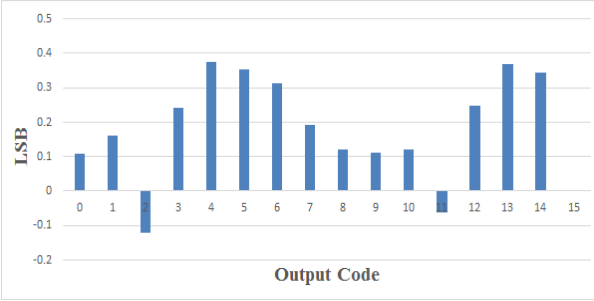

Fig.6: DNL Plot Of Proposed ADC From 0 To 15 Codes

Fig.5 and Fig.6 shows the INL and DNL values for Codes from 0 to 15. For the proposed ADC, you can see the maximum INL of 0.35LSB and DNL of 0.38LSB.

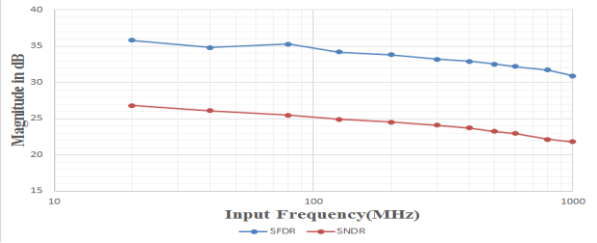

Fig. 7: SFDR And SNDR Plotted Versus Input Frequency

The proposed ADC output digital codes are given to the input of Ideal DAC and then the input analog waveform is reconstructed. For the reconstructed Sinusoidal waveform, we have calculated FFT. From the FFT plot the observed SFDR is 34.2dB and the SNDR is 24.92dB. In Fig. 7 you can see the SFDR and SNDR plotted with different input frequencies.

IV. CONCLUSION

In this paper a 4-bit Flash ADC by employing Binary search algorithm is proposed. This is going to useful in high speed and low power applications like ultra-wideband and Optical communication systems. The proposed ADC requires 7 comparators for 4-bit and if you increase the resolution to 5-bit then you require two more comparators and so on. So, which saves huge amount of power and chip area also. The calculated INL and DNL are 0.35 LSB and 0.38 LSB respectively. And the design consumes 242uW power and the Sampling frequency of the proposed ADC is 1.5 GS/s. The SFDR of the ADC is 34.2 dB and SNDR calculated from the FFT of the reconstructed signal is 24.92dB.

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Table1: Adcs Summary Comparison

Author Name	Rabuske [2]	Sundstrom[4]	Tousi [5]	Poulchart [6]	Manoj [7]	This paper
Technology (nm)	90	90	65	45	45	14
Supply voltage (V)	1.2	1.2	1.2	1.05	1.2	1.0
Power	4.2mW	30mW	2mW	22mW	172uW	242uW
Speed (GS/s)	1.5	2.5	1.2	3.2	1.05	1.5
Resolution	4-bit	4-bit	4-bit	4-bit	4-bit	4-bit
INL (LSB)	-	0.54	+0.78/-0.83	0.17	0.40	0.35
DNL (LSB)	-	0.48	+0.54/-0.38	0.23	0.42	0.38
SNDR (dB)	23.85	22.83	23.2	29.06	-	24.92