Efficient Modified Reduced FFT(MRFFT) Feedback-Commutator Architecture Design

P.Kabilamani[1], Dr.C.Gomathy[2]
[1]Research Scholar, Department of ECE, SRM IST, Chennai.
[2]Professor and Head, Department of ECE, SRM IST, Chennai.

Abstract

In this paper, an efficient MRFFT has been proposed by combining the characteristics of each Radix-2 single delay feedback (R2SDF) and Radix-4 multipath delay commutator (R4MDC).The MRFFT design uses commutator rather than advanced multipliers which reduces latency and the usage of processing elements is reduced which in turn reduces the hardware complexity. In future, the MRFFT design can be used to improve the performances of LTE wireless communication mainly for low coverage area where the signal strength is low. The proposed MRFFT is implemented by using verilog and verified by using modelsim.

Keywords - *MRFFT, Radix-4 multipath delay commutator, Radix-2 single delay feedback,OFDM.*

I. INTRODUCTION

Non programmable algorithm-specific processors are used for the calculation of FFT algorithms. They are mainly used for fixed length FFTs. It's so optimized with regard to memory structure, management units and process components. The algorithmic-specific processors are classified mainly into three types. They are column FFT processors, parallel FFT processors, pipelined FFT processors. The above mentioned processors completely display the various mapping of the signal-flow graph.

Consider 8-point; totally parallel FFT needs twenty four advanced adders and five advanced multipliers. The hardware demand is more and therefore not power economical. To scale back the hardware quality, pipelined FFT or a column is used. A collection of process components in an exceedingly column FFT processor reckon one stage at a time. For computing the output, the results are given to same processing elements. For longer length, the routing for the process components is advanced and tough.

In pipelined FFT processor, every stage has its own set of process components. As soon as the inputs are available, the processor will calculate the data. The above mentioned processors have options like simplicity, high outturn and modularity. These options are vital for real time application wherever the signals are given in the logical order. Therefore, we choose pipelined design for MRFFT processor implementation.

II. RELATED WORKS

FFT is enforced as software system, general purpose digital signal processor, application specific processor or recursive specific processor. In [1], Radix-2 single delay commutator (R2SDC) FFT was projected. In this, commutators are used to acquire signals in frequency domain. R2SDC FFT was performed using verilog and it provides additional information quality compared to traditional FFT. In [2], changed Radix-2^5 booth algorithmic program is employed. In this, System on Chip (SOC) was enforced for MIMO-OFDM transceiver design for software system outlined radio (SDR) design. The hardware based FFT is designed using Xilinx virtex-5 FPGA based ADRES reconfigurable processor. In [3], 64 point FFT is computed for real time application with reduced latency. In [4], the projected FFT reduces the usage of advanced multipliers from 176 to 128 and also the hardware quality is reduced in comparison with existing mixed number FFT by 2 hundredth. In [7],the projected processor is used to reduce the hardware required by chip and it is capable of reducing the memory usage which provides power utilization. In [8], the combined SDC-SDF designs are projected to reduce complex multipliers and processing elements. It is suitable for single delay path FFT processors.

This work has been focusing in reducing the amount of advanced multipliers and butterfly components for FFT computation. Proposed MRFFT has been designed in Verilog and simulation is determined exploitation Xilinx ISE.

III. PIPELINED FFT ARCHITECTURE

Pipeline design utilize multiprocessing among the stages. The final structure accommodates one processing element between commutators at every point. The operation of butterfly is subtraction and addition of the input. The commutator is sort of a switch to rearrange the information from the processing element in order to perform subsequent calculations more easily.

This design is used to achieve high speed operation. The matter with this design is that the comparatively giant die area is needed by the (log N) processing elements. Pipelined design is categorized into 3 groups:

- Single path delay feedback(SDF) design
- Multipath delay commutator(MDC) design

- Single path delay commutator(SDC) design

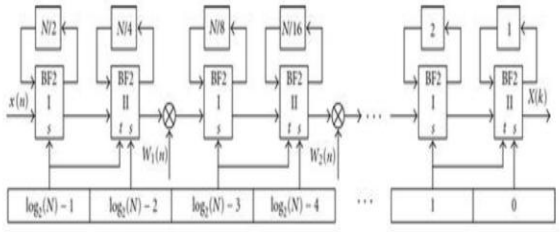

Figure 3.1 Pipelined Architecture of FFT

IV. SINGLE PATH DELAY FEEDBACK(SDF) ARCHITECTURE

In this design, the input passes through only one path. The processing element performs the computation on the information. The output from the processing elements is stored in memory or registers. Because of using a single output path, one advanced multiplier factor is needed for this architecture.

A. Radix-2 Single Delay Feedback (R2sdf) Architecture

The feedback mechanism is introduced to attenuate the number of delay elements. During this design, once the input is given to the butterfly structure, only half the amount of outputs from every stage is given to the input buffer. This design is named Radix-2 single path delay feedback (R2SDF).

Before the computation starts, the delay components at the primary stage save 1/2 the input samples. Throughout the execution, the processing element of primary stage store one output and next output is instantly given to following step. Therefore, within the new temporary frame once the delay components are crammed with contemporary input sample, the outputs of the preceding frame is given to following stage. The processing element acts as feedback loop in this architecture.

When the multiplexer input is zero, the butterfly is inactive and information passes by. Once the multiplexer input is one, the processing element processes the incoming data. Because of using feedback system, we tend to cut back the necessity of delay components from 3N/2 to N -1 (N/2 + N/4 +... + 1) that is negligible. The amount of multiplier factor is precise similar as R2MDC FFT design, i.e., log 2(N)-1. The employment of multiplier factor and processing elements are 50%. The 64 point DIF R2SDF architecture is shown in figure 4.1.

B. Radix-4 Single Path Delay Feedback (R4SDF)

Radix-4 single-path delay feedback (R4SDF) may be a modified form of R2SDF.In radix-4 algorithmic program the amount of multipliers is reduced to log4(N)-1 compared to R2SDF. The usage of the processing elements is 25%. The radix-4 SDF processing elements becomes more complex than the radix-2 SDF. A 64-point DIF R4SDF FFT is shown in Figure.4.2.

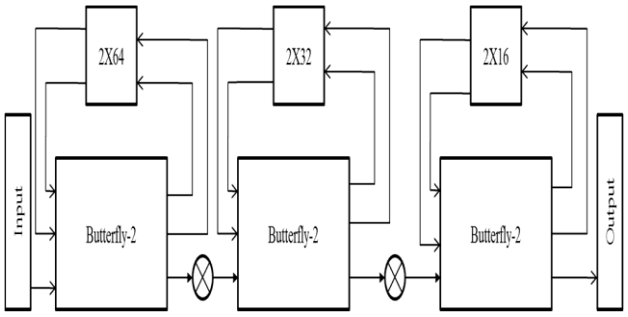

Figure 4.1 64 Point DIF R2SDF Architecture

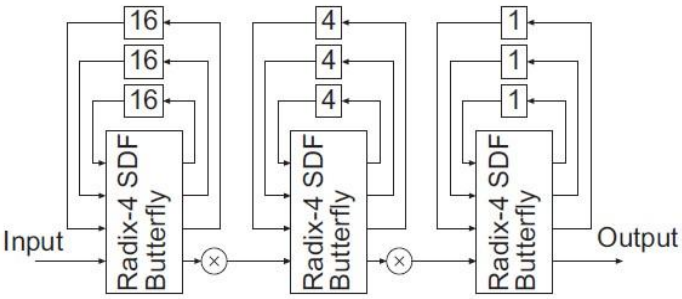

Figure 4.2 64-Point DIF R4SDF Architecture

V. MULTIPATH DELAY COMMUTATOR(MDC) ARCHITECTURE

In general the multipath delay commutator, the inputs are given in a parallel manner. The data enters into the commutator with appropriate delays and processing elements are used for performing data addition at every step. The transitional information isn't given back to register. It's the next outturn rate is more than the single path delay feedback design.

A. Radix-2 multipath delay commutator(R2MDC)

The R2MDC is the best way for implementing the radix-2 FFT algorithmic program employing a pipeline design. R2MDC FFT for 8 point is given in the Fig 5.1

When a frame arrives, the primary half inputs are multiplexed to the top-left delay components and the remaining input samples are fed into the butterfly. During this, the primary input is delayed by four samples and enters into the processing elements at the same time with the fourth input sample. It completes the first step of the pipelining process. The multiplier factor and output from the first stage of butterfly element is given to the MDC between first two stages. They have delay components (multipath) and one commutator. The MDC ease the information dependency downside. The 1st and 2nd stage outputs from the top of the

processing element are given to the two higher delay components. Then, the switch changes and also the 3rd & 4 th stage o/p are given to the second stage of processing elements. The 1st and 2nd stage o/p from the multiplier factor is currently delayed by the higher delay elements which makes them to arrive along with the 5th & 6th o/p.

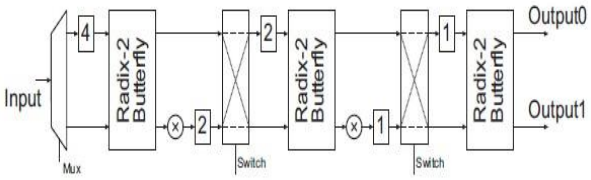

Figure 5.1 8-Point DIF R2MDC Architecture

The multiplier and butterfly remain inactive for half the time and wait for the new inputs. The usage of the multiplier and butterfly is 50%. The number of delay elements required for this architecture is 4 + 2 + 2 + 1 + 1 = 10 for the 8-point FFT. Similarly, for N-point FFT the total number of delay elements can be calculated by $N/2+N/2+N/4+...+2$, i.e., $3N/2$-2.Only one multiplier is required for each stage and the number of multipliers for N-poi nt is log2 (N)–1.

B. Radix-4 Multipath Delay Commutator(R4MDC)

The R4MDC design is comparable to R2MDC. Inputs are separated by a 4:1 mux and (3N/2) delay components at the primary stage. R4MDC is employed between 2 levels which is called stages. The calculation of data will happen only if the last quarter part of information is combined and given to the butterfly. The employment of multipliers and also the butterflies are twenty five. The FFT length must be 4n. A Radix-4 Multipath Delay commutator (R4MDC) FFT for 64 point is given below in Fig. 5.2

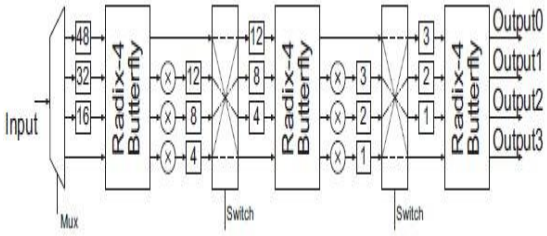

Figure 5.2 64 Point R4MDC Architecture

VI. SINGLE PATH DELAY COMMUTATOR(SDC) ARCHITECTURE

The single delay commutator (SDC) design is predicated on changed multipath delay electrical switch. In every word cycle, each stage produces one output instead of four outputs as in MDC. Every input needs one advanced multiplier factor, a delay commutator and a butterfly part.

A. Radix-4 Single Path Delay Commutator (R4SDC)

To extend the employment of the butterflies, a modified radix-4 butterfly structure is proposed. Within the modified radix-4 butterfly, only 1 output is made as compared with four within the typical butterfly structure. To supply a similar four outputs, the butterfly works fourfold rather than only 1. Attributable to this change, the butterfly contains a utilization of 100 or 4.25 percent. For this transformation we tend to give a similar four input at 4 completely different times to the processing elements. Some additional delay components are needed with this design. The processing element needs signals and commutators. The amount of multipliers is log4(N)-1, that is a smaller when compared with R4MDC FFT design. The employment of the multiplier is seventy five attributable to the actual fact that a minimum of fourth part of the information area unit increased with the trivial twiddle factor one. The architecture of a 16-point DIF R4SDC FFT is given below.

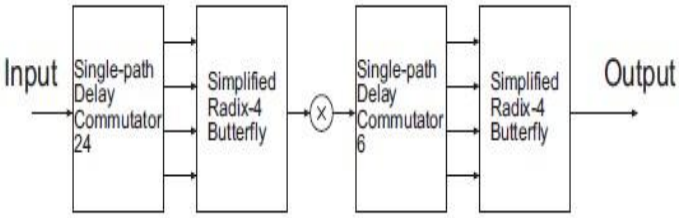

Figure 6.1 16 Point R4SDC Architecture

Advantage of this design is to improve the utilization of butterfly structures. The number of delay elements used is increased greatly is the main disadvantage of this architecture.

VII. PROPOSED MRFFT ARCHITECTURE

In proposed MRFFT architecture, each Radix-2 single delay feedback (R2SDF) and Radix-4 multipath delay commutator (R4MDC) has been combined. The proposed MRFFT will have each the benefits of both R2SDF and R4MDC. The amount of complex multipliers needed for R2SDF is logN-2, the complex adders is 2logN and also the registers is N-1 with base power 2. For R4MDC, the specified range of complex multipliers is 3logN-3, the complex adders is 8logN and also the registers is (5/2)N-4. The utilization of multipliers and adders is 50% for R2SDF and for R4MDC is 25%. The utilization of registers is 100% in case of R2SDC and 25% for R4MDC.

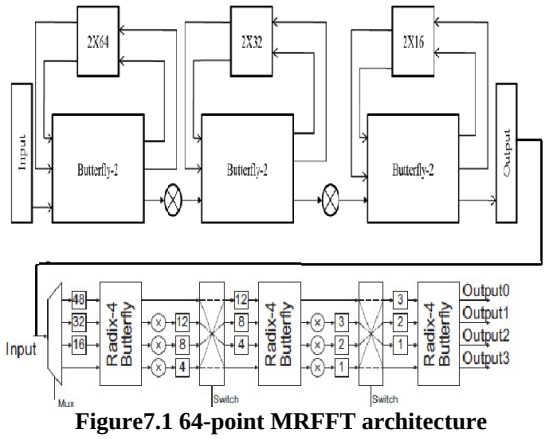

Figure7.1 64-point MRFFT architecture

In this architecture, the output of 64 point radix-2 single delay feedback (R2SDF) is given as the input to Radix-4 multipath delay commutator (R4MDC).

VIII. SIMULATION RESULTS

The simulation result for MRFFT architecture is obtained using modelsim is shown below.

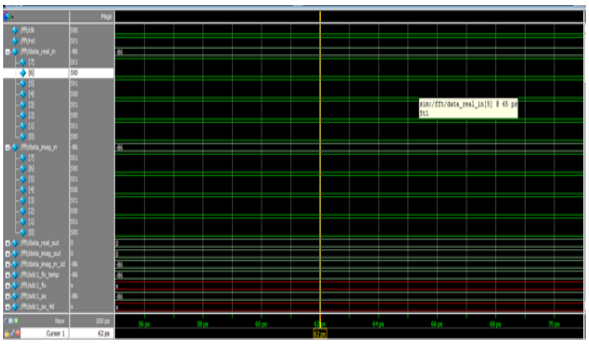

Figure 8.1 simulation result of FFT

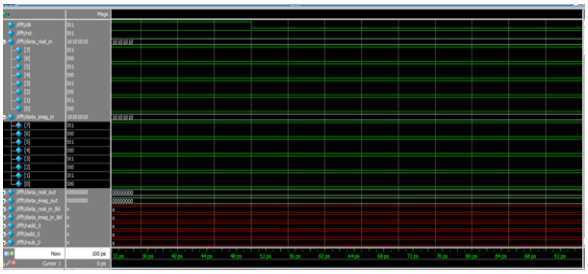

Figure 8.2 simulation result of IFFT

Table-1 Power and Delay Summary

Architecture	Power in watts	Time in ns
FFT	0.041	6.216
IFFT	0.041	22.46

Table-2 Device utilization of FPGA for FFT

Logic utilization	Used	Available	Utilization
Number of slices	804	1920	41%
Number of FlipFlops	681	3840	17%
Number of LUT's	1497	3840	38%
Number of Bonded IOB's	34	141	24%
Number of GCLK's	1	8	12%

Table-3 Device utilization of FPGA for IFFT

Logic utilization	Used	Available	Utilization
Number of slices	1278	1920	66%
Number of FlipFlops	929	3840	24%
Number of LUT's	2428	3840	63%
Number of Bonded IOB's	34	141	24%
Number of GCLK's	1	8	12%

IX. CONCLUSION

In this paper, a Modified Reduced Fast Fourier Transformation (MRFFT) has been designed using Verilog language. The aim of this proposed FFT is to scale the hardware requirements and to consume power efficiently.

REFERENCES

[1] K. Malathy and B. Justus Rabi, " A novel VLSI based Radix-2 single path delay commutator FFT architecture design"

[2] N.Janakiraman, P.Nirmalkumar and Syed Moshin Akram ,"Coarse grained ADRES Based MIMO-OFDM Transceiver with New Radix-2^5 pipeline FFT/IFFT processor".

[3] Ramesha.M, T.Venkata Ramana, "Design and implementation of fully pipelined 64-point FFT processor in a FPGA",Internatinal Journal of Applied Engineering Research,2016

[4] Kim EJ, Lee JH, Sunwoo MH ,"Novel shared multiplier scheduling scheme fo area-effecient FFT/IFFT Processors.IEEE Transcctios on very large scale integration systems".2015 sep;23(9):1689-99

[5] Cheng C, Parhi K. "High throughput VLSI architecture for FFT computation".IEEE Transactions on circuits and systems (II):Express Briefs.2007 Oct;54(10):863-7.

[6] Bhakthavatchalu R,kannan SK,Nirmala Devi M. "Verilog design of programmamble JTAG cotroller for Digital VLSI IC's", Indian Journal of Science and Technology,2015 Aug;8(17):1-79999

[7] Kai-Jiun Yang,Shang-Ho Tsai,Gene C.H.Chuang,"MDC FFT/IFFT Processor with variable length for MIMO-OFDM Systems"

[8] Zeke Wang, Xue Liu, Bingsheng He, and Feng Yu ,"A Combined SDC-SDF Architecture for Normal I/O Pipelined Radix-2 FFT",IEEE Transcation on Very large scale Integration (VLSI) systems,May 2015