Optimized Tsv Based 3d Integrated Circuit For Improve Power With Reduced Area Of Circuit

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Abstract:- The impact of huge coupling capacitance between TSVs on the extension, power and coupling confusion in 3D interconnects likewise offers genuine difficulties to the presentation of 3D-IC. Because of the level of design multifaceted nature presented by TSVs in 3D ICs, the significance of beginning time assessment and streamlining of extension, power and sign respectability of 3D circuits can't be disregarded. The interesting commitment of this work is to create strategies for exact examination of timing, power and coupling noise over different stacked gadget layers during the floor arranging stage. Fusing the effect of TSV and the stacking of various gadget layers inside floor arranging structure will accomplish 3D designs with predominant execution.

Keywords: 3D ICs, Silicon Integrated Circuits, Through Silicon Vias.

I. INTRODUCTION

The main aim of dissertation is to meet the designing issues of 3D ICs by providing additional capabilities to the existing 3D floor planning structure. These TSV-aware capabilities include the importance of TSV location, area and its RC parasitical in early stage of design. The developed floor planning device will facilitate in early stage optimization and evaluation of power, timing and signal integrity of 3D circuits. Early design exploration will enable improved design choice for previous stages in the 3D IC design process; so that the design is merging and comprehensive timing termination might be improved. Most computational systems have rapidly growing memory bandwidth demanding that can be achieved by stacking memory processor block or top of logic.

A memory bus I/O circuit delivering 100 GB/s memory bandwidth would occupy only 2W in 3D integration technology in comparison to 20W in 2D-IC technology [1]. The technique for 3D integration pertinent to this dissertation is TSV-based 3D IC.

II. Through-Silicon Via Technology

A Through-Silicon-Via connection is a dynamic connection between the two sides of a Si wafer that is electrically insulated from the substrate and from other TSV connections [2-4]. The insulation layer surrounding the TSV conductor is called the TSV liner. TSVs are used as interconnect between packages, as an alternative to flip chip and wire-bond methods, allowing for better power and faster performance profile. TSV connecting consecutive device layers occupies silicon area only on the upper device layer. The diameter of fabricated TSVs is typically in the range 2-10μm, and the aspect ratio ranges from 10:1 to 20:1. The basic physical and electrical characteristics of TSVs will be defined by the 3D process flow.

TSV-based 3D Process Flow

The process technology for TSV fabrication is well established and is being manufactured in high volume [4]. The steps for TSV-based 3D process are

(i) TSV formation,
(ii) C wafer thinning,
(iii) Bonding and Alignment.

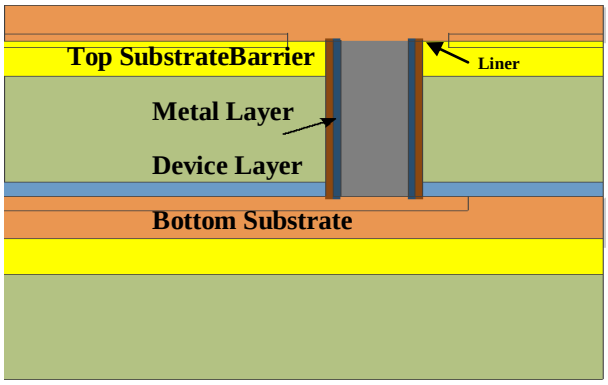

Figure1. TSV design connecting two vertically stacked device layers

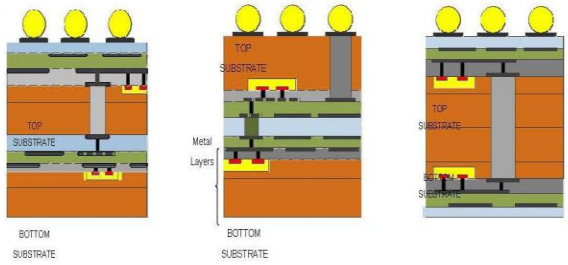

Figure 2: Comparison of different stacking techniques, (a) Face-to-Back, (b) Face-to-Face, and (c) Back-to-Back.

Benefits

3D integration is fast emerging viable design paradigm to solve the previous interconnect congestion [2] encountered in 2D ICs, because of the continued device scaling. Recent advancements in TSV technology hold admirable scope for future generations. The advantages of 3D ICs with TSVs compared to classical packaging processes and two-dimensional SoC can be compiling as follows:

1. Shorter Interconnects
2. Lower Costs
3. Higher I/O Bandwidth
4. Reduce Power utilization
5. Heterogeneous Integration

III. Proposed Methodology

In the proposed approach, we introduce a coupling noise term in the cost function (*CF3)*, which is the summation of noise voltage at each net. The coupling noise term assists the floor planning algorithm in monitoring the influence of TSVs on the coupling noise in the wire. This ensures that the placement of blocks and TSV islands, as well as nets-to-TSVs assignment minimizes the overall coupling noise in the circuit.

Parameters α, β and γ represent the weights associated with the cost function parameters.

During 3D floor planning, the direct optimization of coupling noise can play a decisive role in reducing coupling-related SI issues. This early optimization may not completely eliminate the noise, but will assist in reducing the magnitude of coupling noise and number of violating nets.

Diagonal TSV Arrangement

In a TSV island, the position of a TSV with respect to other TSVs, plays a significant role in determining the overall coupling noise. In a regular array the TSVs in the middle of an island will have worse coupling due to eight neighboring TSVs, shown in red. The TSVs shown in yellow are surrounded by 5-TSVs, and will have sidewall coupling with 3-TSVs and diagonal coupling with 2-TSVs. The TSVs at the corner of the island, shown in green, will have the least coupling, with only three adjacent TSVs.

In any case, receiving with RPR in should even now pay additional zone overhead and power utilization.

The previous connection methods for 3D ICs are wafer-to-wafer, die-to-wafer and die-to-die bonding.

The W2W bonding offers low cost, higher via density and improved alignment. So, W2W suffers from low output as bad die can be stacked on top of a good die resulting in chip failure. D2W and D2D result in higher output as the dies are tested prior to 3D stacking [5-7]. The additional lower throughput and testing cost can increase the overall cost of the chip.

In addition to these primary characteristics, three secondary characteristics are identified, as Face-to-Back, Face-to-Face and Back-to-Back. This paper is based on F2B die-stacking strategy, as it does not limit the number of device layers that can be stacked.

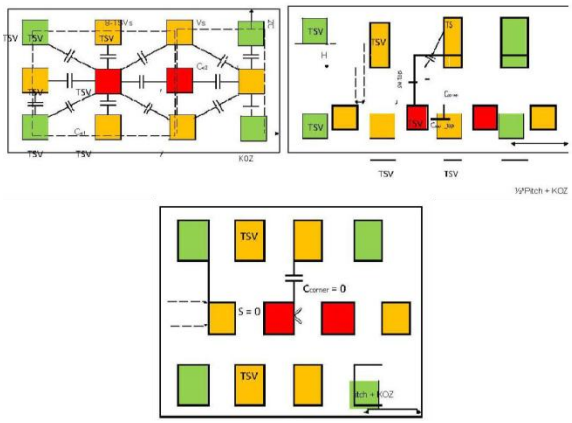

Figure.3: Different TSV-to-TSV coupling capacitance inside a TSV island consisting of middle-TSV (red), row-TSV (yellow), corner-TSV (green) for (a) Regular arrangement, (b) Diagonal arrangement (Pitch > 2*Diameter), (c) Diagonal arrangement (Pitch = 2*Diameter)

For the purpose of the analysis of diagonal TSV arrangement, it is assumed that the TSV pitch is equal to four times its diameter. By having larger TSV pitch, we ensure that *Ccorner* is not equal to zero in the diagonal arrangement. The capacitance of TSVs inside the island decreases by 9%-14% for regular TSV arrangement. The capacitance of corner, row and middle TSVs for diameter 2µm and pitch 4µm is 7.23fF, 9.12fF and 11.93fF respectively.

The TSV-to-TSV coupling component for corner, row and middle TSVs in the regular arrangement for 4µm TSV pitch is 3.03fF, 4.97fF and 7.87fF. The worst coupling capacitance of TSVs remains constant for island sizes larger than 2x2. All the TSVs in a 2x2 island will be corner-TSVs with capacitance of 6.56fF and 5.94fF for regular and diagonal arrangement respectively. Therefore, the worst and average TSV capacitance is much lesser for smaller size of islands. As the TSV array size increases, the number of row and middle TSVs increases, causing the average TSV capacitance of the island to rise. In the table, we can see a drastic increase in the average TSV capacitance when the TSV array size increases from 2x2 to 6x6. As the TSV array size increases beyond 6x6, we observed that the average capacitance nearly saturates. The worst capacitance of TSV islands for array size larger than 2x2 represents the capacitance of mid-TSVs, which is 10.87fF and 8.24fF for regular and diagonal arrangement respectively.

Table 1 Average and worst coupling capacitance for different TSV array dimensions inside island, TSV diameter = 2µm, height = 20µm and pitch = 8µm

TSV	# TSVs			Regular Arrangement			Diagonal Arrangement		
array	Cor	Row	Mid		Avg. Cap (fF)	Worst Cap (fF)		Avg. Cap (fF)	Worst Cap (fF)
2x2	4	0	0	Cor	6.6	6.56	Cor	6.1	6.09
4x4	4	8	4	(6.56fF)	8.3	10.87	(6.09fF)	7	8.47
6x6	4	16	16	Row	9.1	10.87	Row	7.5	8.47
8x8	4	24	36	(7.88f)	9.5	10.87	(6.76fF)	7.7	8.47
10x10	4	32	64	Mid	9.7	10.87	Mid	7.8	8.47
12x12	4	40	100	(10.87fF)	9.9	10.87	(8.47fF)	7.9	8.47

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The TSV pitch for this experiment is kept four times of its diameter. This will increase the size of TSV islands, influencing the chip area and wirelength. But, for fair comparison between regular and diagonal TSV arrangement, we want to keep TSV pitch the same. We have used CF2 during the floor planning and the coupling noise is evaluated on the final floor plan. The tables show the number of nets in the specified noise range, the total and worst coupling noise in the circuit. It can be seen that the number of nets with noise voltage exceeding 0.1V (Vnoise > 0.1) reduces significantly for diagonal TSV arrangement. This suggests that the diagonal TSV arrangement reduces the magnitude of coupling noise introduced by TSVs significantly by reducing TSV sidewall coupling capacitance. Although the number of nets with noise voltage below 0.1V increases for diagonal TSV arrangement, but their impact can be ignored as the threshold voltage of the CMOS transistors in 45nm technology is around 0.12V–0.3V [8]. The diagonal TSV arrangement reduces total and worst coupling noise by up to 30% and 21% respectively. The coupling noise due to worst TSV capacitance is higher than with the average TSV capacitance by up to 32% and 19% for TSV diameter 1µm and 2µm respectively. The coupling noise due to average TSV capacitance will be a better approximation of total coupling noise, as not all the TSVs would have coupling from all the sides. Since, the TSV-to-TSV coupling capacitance for diagonal arrangement has not been verified with the simulations, the presented results for the coupling noise in the interconnects are just an approximation.

Buffer Insertion by using Wire Capacitance-aware

There we show a comparison of TSV-aware buffer insertion and wire capacitance-aware buffer insertion schemes. Both the methods are utilized on the final floor plan after calculate the interconnect density on particular device layers [9].

TSV-aware buffer insertion scheme presented in previous optimizes buffer insertion for particular nets, and only accounts for the units of TSVs and their RC parasitics. But it ignores the different capacitance of segments of a 3D wire routed on different device layers.

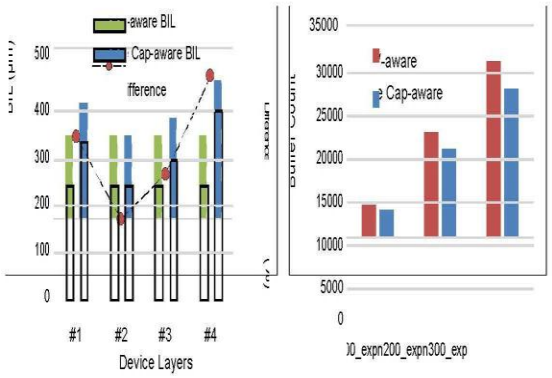

Figure 4: (a) Optimized buffer insertion length using TSV-aware and wire capacitance-aware buffer insertion ength, (b) Total number of buffers in modified GSRC circuits using TSV-aware and wire capacitance-aware buffer insertion approach, TSV diameter 2µm, buffer and wire parameters

The total units of buffers in the wires are determined by the length of buffer insertion. TSV-aware BIL doesn't take into account the eccentric interconnect density, resulting in the same *BIL* on every device layer.

CONCLUSION

Through silicon via based 3D incorporated circuits have raise a new design worldview which investigates the vertical measurement, so as to minimize the exhibition and power detention related with long interconnects in 2D circuits. TSVs empower vertical interconnects crosswise over stacked and reduce stimulation the bucket in 3D-IC design, bringing about decreased wire length, quicker speed, impression, improved data transfer capacity and less directing blockage. Be that the impact of TSV area, position and electrical qualities on the 3D interconnects isn't immaterial and must not be overlooked.

In this work, we introduced an early structure investigation approach utilizing created 3D floor planning instrument for progressively exact and practical assessment of execution, power, and coupling noise in the 3D ICs. Additionally, arrangements are exhibited which help to accomplish 3D formats with clean planning, power and assurance honestly thinking about the allotment of wires and TSVs on the design.

FUTURE WORK

An accurate criterion of TSV and wire RC parasitic within the 3D floor planning structure simplify better design decisions for later stages in the 3D IC design flow, so that the overall design convergence and timing closure can be better achieved.

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