A Review on Low Power Memory Design Technique

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Abstract

This article describes the 10L Ultra Low Power Static RAM (ULP) for Internet Object (IoT) applications running below the threshold. The proposed SRAM, as a rule, operate at low supply voltage with a high static and dynamic noise margin. IoT applications require a battery compatible low leakage memory architecture in the lower threshold region. Therefore, to improve leakage energy consumption and cell stability, this technical document presents the reliable SRAM 10T power system. The proposed cell uses a p-MOS transistor with a power system to reduce power leakage or static power in standby mode. Also, due to the overlapping of the n-MOS transistor in the 10T SRAM latch and the separation of the read path of the 10T SRAM latch, static and dynamic noise reserves in reading and write operations show significant tolerance. There are variations in the process parameters, voltage and temperature (PVT) of the device. The proposed SRAM significantly improves leakage power, static noise reading (RSNM), static noise recording (WSNM), write capacity or write trigger point (WTP), read-write power and dynamic read field (DRM) show performance. Also, these parameters of the proposed cell are observed in 8 kilobits (KB) of SRAM and are compared with the existing SRAM architecture. Based on the Monte Carlo simulation results, it was found that the leakage power of the proposed low SRAM LVT 10T threshold is decreasing.

Keywords: *Memory design; Ultra power; Circuit design*

I. Introduction

Latest generation automatic power without contact or connection Objects must develop a platform with very low consumption. These devices have batteries or antennas. Data exchange with the reader Energy. For non-contact smart card applications, Integrated into a small form factor to reduce energy Can be used with devices. So to ensure proper operation For devices with acceptable performance Significantly reduces overall energy consumption. The main contributor to energy consumption is non-volatile embedded technology. Memory (e-NVM) Read, delete, and Scheduling tasks.

II. Low power memory design

Morirnura et al.[1]analysedultra-low-power 1V SRAM circuits technology has been described for word-wise configurable memory macrocells. With modified address allocation, a shared bit line is proposed to zero the current of the waste storage cell by removing the loss of the SRAM cell architecture field. For the new design of the SRAM cell, we have prepared a bit line precharging scheme with multiplexer combined charge transfer amplifier for high sensitivity read operations and equalisation lines for duty recovery operations at high speed. The 64kb (2kw x 16b x 2) test chip used to operate in 1-V mode was designed using the 0.35µm multiple threshold voltage CMOS logic (MTCMOS) process. With an increase of about 13%, the SRAM macrocell with traditional I-V word configuration has an analogue consumption of 1/4 (486 FW).

Lee.[2]stated thatThis document describes the design of a pseudo-asynchronous SRAM 0.9V, Llnsec, multiport, consisting of a single READ bit line and a single WRITE bit line for each port. The SRAM uses a new memory cell with a self-winding wave-tube technology architecture to increase speed and reduce power consumption. Each SRAM cell contains a predefined transistor that defines the contents of the memory word for all. This allows all records to be written by writing "0" on the appropriate bits. Each SRAM memory cell also has a step-down transistor as a buffer that unloads the pre-bit bit line to read "0". Therefore, writes in memory require a single write bit line and a single read bit line as described in Table 1.

Thomas et al.[3]studied ultra-low SRAM (ULV) circuit design techniques and digital circuits based on partially excluded insulators (SOTs). There is a systematic design methodology dedicated to SRAM memory cells, which takes into account the effect of the floating body at different levels of the design process. This method is used to design a new memory cell with 4 auto-refresh transistors and a comparison of

6 transistors. ULV digital circuits are studied, ranging from essential ports to complex wavelet transformations. It has been shown that for partially depleted 130 nm SO1 technology, the use of high-speed transistors results in a significant improvement in speed and energy savings. The energy-delay product is multiplied by 2.4.

Levacq et al.[4]designed the new CMOS digital storage device is based on the combination of two reverse-biased composite CMOS diodes, each with very low leakage and negative reverse-mode impedance characteristic. The polarisation of MOS transistors in very low inversion, with negative gate-to-source voltages, generates a lower static current than the magnitude lower than conventional cross-coupled CMOS inverters. Based on our device, the 7 transistors of the SRAM cell shown.Modelling, simulation and experimental characterisation of the main properties of this cell described for a partially depleted SOI CMOS process of 0.13 µm. The feasibility of shallow leakage memory circuits is demonstrated experimentally by the design of a 256-bit SRAM column.

Rahman et al.[5]stated that Maintaining the trend of performance evolution and cell stability is a significant challenge for SRAM CMOS in technologies below 20 nm. These challenges come mainly from the fundamental limitations of MOSFETs and doping requirements, as well as from dimensions based on rigid SRAM devices. In this article, we propose a new FET-based volatile architecture synthesizer tuner (TNRAM), called by the FET site integration with ultralow tunnels (TFET) in a new style, circuit, challenge of the scaling of the SRAM CMOS triggers. It is designed to work with uniform type transistors to eliminate nanoscale sizing requirements of the devices and has been adjusted to avoid Static RAM stability issues. Analytical projections show significant performance benefits. The TNRAM 6T has an active power of fewer than 4.38 times and a power dissipation 174 times lower than that of the SRAM HP 6T in the 16 nm technology node.

Ngueya et al.[6] stated that Deficient power and high-performance voltage sensing amplifier are shown Based on the recirculation of charge between a tank capacitor and the parasitic bit line capacitor, a reference voltage generated dynamically, and the storage pre-charge step starts at the half of the supply voltage. The convocation and the activation of the word line are independent, thus avoiding additional consumption due to the direct path between the power supply and the ground during the preload. The proposed circuit is implemented using 55nm high voltage CMOS UMC technology with a 1.2V power supply. The simulation results show a read access time of approximately 20.6 ns and average power consumption of 0.56 µW / MHz / bit under typical operating conditions at 27 ° C.

Kim et al.[7]stated that with incredible CMOS technology, the stability of SRAM data at extremely low power voltage had become a critical issue for portable system applications. In this article, we present an advanced SRAM 8T that can work well-sublimed voltage regime. The bit cell uses a differential equilibrium in the read and writes paths and allows an efficient interleaving structure of the column. In the read operation, the help column of the cell column determines the cell to be unaffected by the interruption of reading. Additionally, the bit cell maintains the "low" node voltage of vulnerable data near the ground during a simulated read operation, producing almost ideal voltage transfer characteristics essential for robust SRAM functionality. During write access, the spoken word line makes it easy to change the contents of the memory bit. The results of the 180 nm CMOS implementation show that the proposed SRAM is not affected by reading disturbances while providing simulated reading stability of 59.8% and recording capability 3.7 times greater than a threshold compared to conventional SRAM 6T.

Schiavone et al.[8]analyzedend points of the Internet of Things (IoT) require extreme energy efficiency coupled with a wide range of energy performance operations. Thoroughly exhausted SOI (FD-SOI) is an attractive technology for low energy consumption and offers high performance for power, performance and surface adjustment (PPP) at design and execution time. This article discusses Quentin: an open-source 32-bit MCU RISC-V SoC with an autonomous I/O subsystem optimized to support the range of sensors in IoT terminals coupled to an optimized processor for neighboring environments. Threshold calculation and heterogeneous memory architecture are described (standard cell and SRAM) for better operation of 22nm FDX low voltage capacities. The system executes up to 2,400 million RV32IMC equivalents per second (MOPS) and achieves the best power density of 6 µW / MHz for energy efficiency of 433 MOPS / mW.

Khodja et al.[8]stated that the goal of this work is to set up a network of artificial neurons in the FPGA Forum. This implementation aims to provide hardware integration solutions in areas such as monitoring, diagnostics, maintenance and control of power systems and industrial processes. The Similink library created by Xilinx contains all the blocks needed to

create artificial neural networks, except several functions. The sigmoid function in this work, the proximity of the polymorphic form approximated. Subsequently, the sigmoid functionality was implemented using the Xilinx library in FPGA. The test results are satisfactory as described in Table 1.

Table. 1 Literature survey

Year	Publication	Proposed Methodology	Parameter
Woo et al. [9]	IEEE (2019)	MOSFET	Synaptic device using a floating fin-body MOSFET with memory functionality for neural network.
H. Lee [2]	IEEE (1999)	SRAM	Design of ultra-low power pseudo-asynchronous SRAM.
Y. Ota, Bogdan, and M. Wilamowski[10]	IEEE (1999)	CMOS	Analog Implementation of Pulse-Coupled Neural Networks.
F. Moradi, D. T. Wisland, H.M. ahmoodi [11]	IEEE(2010)	SRAM	SRAM design using body bias technique for ultra-low power.
D. Khodja, A. Kheldoun,[12]	IEEE(2010)	ANN FPGA	Sigmoid function approximation for ANN Implementation in FPGA Devices.
J. Chen, K. S. Chong, B. H. Gwee[13]	IEEE(2010)	SRAM	ultra-low power asynchronous quasi-delay-insensitive (QDI) sub-threshold memory
H. P. Rajani, H. Guhilot[14]	IEEE(2011)	SRAM	SRAM for ultra-low power deep submicron cache memories.
P. D. Schiavone, D. Rossi, A. Pullini[8]	IEEE(2019)	SOC SRAM	Ultra-low-power (ULP) PissimoSoC(system on chip).
N. Saini and G. Saini[15]	IEEE(2019)	SRAM	Circuit Design of Ultra-Low Power Applications.

Proposed Methodology

- Energy and area efficient implementation of Artificial Neural Network (ANN) as shown in Fig. 1.
- Tool Used- Xilinx Vivado, Language- VHDL.
- Implementation- Core neuron circuit with efficient multiply and accumulation unit and activation function.
- Reduced supply voltage.
- Adiabatic switching and charge recovery.
- Logic design for reduced activity.
- Multi-threshold gates.

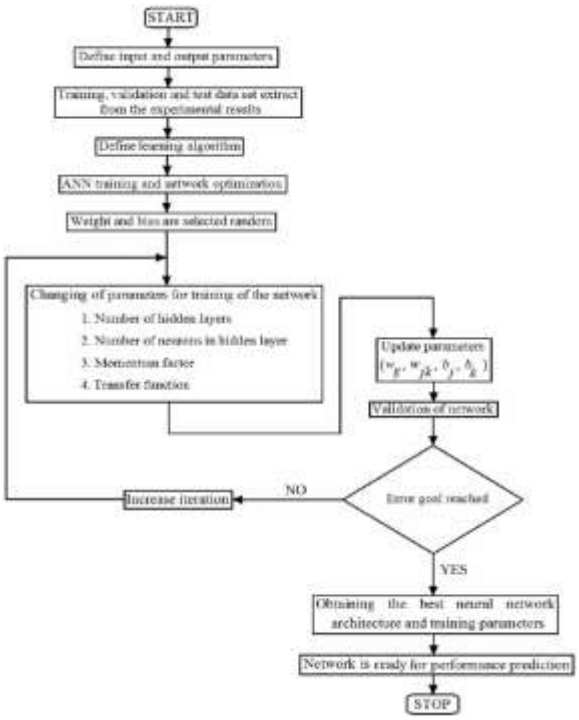

Fig. 1 Flow chart of ANN

III. Expected Outcome's

- Power consumption is critical in today's embedded systems.
- Emerging low power applications include battery-powered internet of things (IOT) sensor nodes, wearable, and medical electronic devices that are power and energy-constrained.
- The memory requirement can be fulfilled by several memory technologies available in the market.

IV. Future scope of the work

- We can use this device in smart projects such as spy-drone, garbage collection, traffic control, and defense.
- Decrease consumption of power.
- Use of cooling capacity will decrease due to compactness of system.
- Increase efficiency of vigilance.

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