Comparison between the performance of the Simulated Annealing and Genetic Algorithms in Physical Conductor Orientation within FPGA

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ABSTRACT: *Reducing the number and length of physical conductors is an important aspect of circuit design, and is the core of systems using SOC (System on Chip) technology. The research presents a comparison between the performance of the Genetic Algorithms and the Simulated Annealing algorithm in the process of arranging the elements and paths of electronic circuits used in the chip (Field Programmable Gate Array FPGA). The research presents the most important points of comparison and guidance criteria for each of the two algorithms in terms of the number of conductors and processing time.*

keywords : *FPGA ، Simulated Annealing , Genetic Algorithms*

I. INTRODUCTION

When talking about electronic designs shown using the FPGA chip, we are talking about millions of electronic elements per design, which requires routing algorithms and positioning of the elements to ensure the design of the best physical design conditions and achieve new conditions, including the abbreviation of the elements used, reducing the number of physical paths, which work On reducing the energy consumed, reducing thermal losses which makes the issue of routing very important.

II.THE IMPORTANCE OF RESEARCH AND ITS OBJECTIVES

The solution of the physical problems of logic circuits (such as reducing the area allocated to electronic masses, reducing the physical paths carrying logical values between blocks, and thus the actual energy consumption and reducing the economic costs associated with manufacturing costs) aims to provide a comparison between the performance of the Genetic Algorithms and Simulated Annealing algorithms.

III. RESEARCH METHODS AND MATERIALS

The research is based on the use of FPGA chip and programmed using VHDL language so that the comparison includes the number of logical blocks and physical paths related to electronic design based on FPGA, which is the material of the research. The results were taken from Quartiz program because the results of the program are able to show the change in the order of blocks and physical paths. Routing algorithms are written using the tcl file that controls the VPR package.

IV. REFERENCE STUDY

Adewole A.P. Egunjobi T.O., Otubamowo K., conducted a comparison between the performance of the two algorithms Simulated Annealing, Genetic Algorithm in solving the mobile vendor statement entitled A Comparative Study of Simulated Annealing and Genetic Algorithm for Solving the Traveling Salesman Problem

V. ELECTRONIC STRUCTURE OF FPGA CHIPS

Programmable digital gate arrays are integrated circuits consisting of arrays of logic gates. Each gate can be configured from one type to another, for example from AND to NAND and NOR to NOT. Figure 1 shows the overall shape of the FPGA system.FPGA chips are solidly programmable, meaning that we can program them to get any logical function using VHDL [3]. One of the most important advantages of FPGA in addition to its low cost is that it provides great flexibility in design and the ability to reprogram it. [1]

In terms of design, FPGA consists of a set of blocks, which perform a range of functions, including transport, including switching and logical blocks (1)

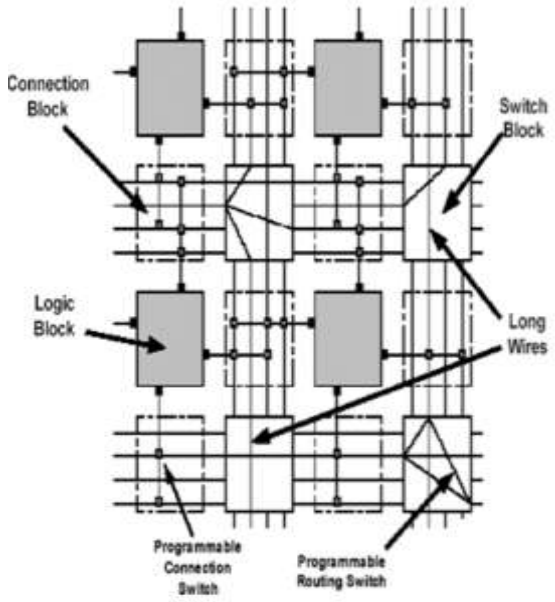
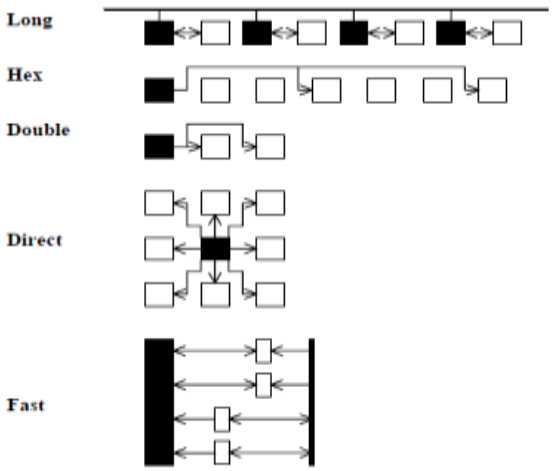


Figure 1 Design structure for FPGA chips

VI. PHYSICAL PATHWAYS USED TO CONNECT BLOCKS IN FPGA

The construction of electronic designs using FPGA relies on the integration of heterogeneous resources, "different types of blocks," which put additional constraints on the routing process in FPGA [4].

Where the placement and routing algorithms are the basis of the physical structure of the programmed design and the main objective is to predict and repair the problem of delay communication between blocks and reduce energy and thermal dissemination [4].Figure (2) shows the types of physical paths that can be used in the construction of electronic designs, which achieve the link between the logical units CLbs (configurable logic block) where (white boxes refer to CLBs and black boxes indicate paths breakers). Long lines span the entire area of the chip, hex lines direct signals to six CLBs and in four directions, Double lines direct signals to the first or second logical units or can be routed in the four directions, direct lines transmit signals between adjacent units Highways are local links to CLBs. The Hex, Double, and Direct lines are similar to the time delay [4].



Figure(2) Physical pathways in FPGA

VII. ROUTING IN FPGA

The structure of the FPGA and its routing paths are quite different from the ASIC designs. Their differences lie in the existence of long networks in FPGAS circuits that connect spaced CLBSs with little time delay. On the contrary, the physical distance and delay between the two units is the truth inherent in ASIC designs,

FPGA physical design tools should therefore be fully informed in the physical design of transport paths [2] due to long path problems caused by the use of more block blocks.

The modern FPGA structure includes heterogeneous resources, which are distributed to FPGA parts. Many modern positioning techniques rely on the principle of division as their basis. At each step of positioning algorithms are also divided into smaller sub-regions and then the circuit is divided into smaller sub-circuits and allocated to sub-regions [2]. For each subregion, a smaller sub-circuit has been set to correspond to it, this division continues until the areas are small enough, dividing the circuits into sub-circuits should balance the resources used in each sub-circuit with the resources available in each sub-region [5] .

VIII. GENETIC ALGORITHM

An algorithm is a set of sequential instructions that aim to solve a problem or accomplish a specific purpose .

Genetic algorithm is a method of random search used in computing to identify the best or closest solutions to the optimal solution from the range of possible solutions that constitute the so-called research space through a series of steps based on comparison and finding the "distance" between solutions and then select solutions Appropriate and reliable in the formation of other solutions (second generation) more appropriate and closer to the optimal solution.

Although genetic algorithms differ by evolutionary computing branches, they share at least the following elements :
chromosomes of Populations: Representing the Space Search, which is a set of problem solutions.

Selection or election: Choosing the Suitable chromosomes as "parents" to mate, but this selection process is not random, but depends on the fitness of the chromosome.
Fitness : A coefficient that gives each chromosome a certain value indicating the efficiency of the chromosome (its approach to the solution), and therefore the selection of chromosomes.
Transit : After selecting the appropriate first-generation chromosomes, the transit through which new chromosomes (new offspring) are formed depends on the native chromosomes.
Random mutation : after the formation of new offspring mutations (changes in their chromosome form) are created, and this helps in reaching the solution faster

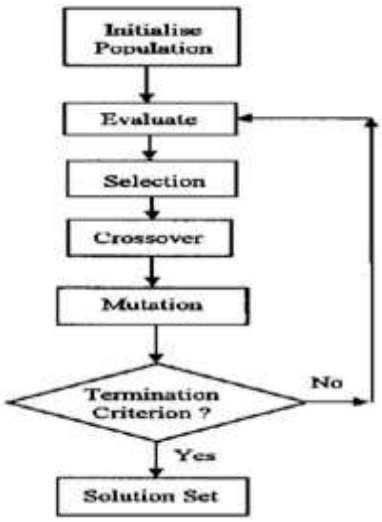
Fitness function
It is a mathematical function used to determine the fitness of the chromosome, usually the best solution (chromosome) is that the fitness function value is greater or smaller depending on the type of problem.

$$\text{Fitness function} = 1/|x + y + z - t| \quad (1)$$

VIII. I. Working mechanism of Genetic algorithms
When we determine the matter to be solved, the algorithm begins its work according to the following sequential stages:

1) Primary Population Census : At this stage, the algorithm forms a set of n chromosomes, each consisting of a l-gene (squared). These chromosomes represent a set of primary solutions to the problem.
2) We determine the fitness function for each chromosome of the census, and then the algorithm calculates the efficiency of each chromosome separately .
3) The algorithm repeats a set of processes until a new strain is reached, these processes are as follows

•Selection begins where a pair (s) of the current population are selected, depending on the mathematical probability value (pS) that is proportional to the efficiency function, if the optimal value of the solution is max or inversely - if not - The same chromosome can be selected more than once.
•The transit procedure is called where a point of the parent dyes is determined according to the probability valueof the transit and then the transit takes place based on that point. If the algorithm is unable to determine thetransit point, the two child dyes
•In some cases, more than one crossing point may be selected
•Mutations get each gene from the two new dyes with a Pm probability by changing the gene value to a different new value to increase the chance of approaching the optimal solution, and then placing the new dyes in the new census.
•After repeating the previous operations, we have a new n chromosome, and here if n individually chromosome is randomly eliminated from the census.
4. After the implementation of the genetic algorithm, the previous census is replaced by the current one.
5.Finally, operations are repeated starting with process 2.
Each repetition of this process is called generation, and the group of all generations is called run. At the end of each operation, there is often one or more chromosomes that are highly efficient compared to their generation.



Figure(4) Box diagram of the genetic algorithm

IX. SIMULATED ANNEALING ALGORITHM
The algorithm in the placement process depends mainly on the temperature so that it calculates the temperature of the adjacent masses and then directs the position based on the cost-function temperature dependent and the steps of the algorithm are as follows:

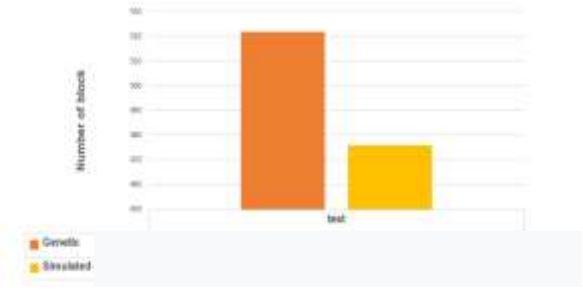
```
old_cost = cost(placement);
for (temp = max_temp; temp >= min_temp; temp =
next_temp) {
for (iteration = 0; iteration < max_iteration;
iteration++) {
Swap random pair of logic blocks;
new_cost = cost(placement);
if (old_cost < new_cost)
if (random >= Func((old_cost -
new_cost)/temperature))
undo_move();
else old_cost = new_cost   /* Keep new placement */
}
}
```

X. APPLICATION AND RESULTS

In this section we will compare the results of the two algorithms and the diagram shows the results of the application of the algorithms to the temperature monitoring system.

Scheme 1 shows the results in terms of the number of logical blocks created in the chip by the two algorithms.

Scheme 1 compares the number of logical blocks used by the chip



From the previous chart, the genetic algorithm has reduced the number of logical blocks (electronic elements used in building design using FPGA chip). This is due to the fact that the proposed algorithm has changed the method of ordering from memory and thus has been modified in the physical path distribution method in the chip, allowing the possibility of achieving higher utilization of the block block.

XI. CONCLUSIONS AND RECOMMENDATIONS

we concluded that shortening the logical blocks and blocks in FPGA chips is one of the most important aspects that should be taken into account when designing systems using FPGA.Through the work, the performance of the genetic algorithm was compared with the Simulated Annealing algorithm.Because the latter depends on the guidance taking into account the heat only the second took into account the reduction of energy and reduce distances between blocks

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