# Design of Programmable High Speed I/O S

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***Abstract***

*In this paper an attempt is made to design some basic features of a programmable high speed I/O like bidirectionality of I/Os, buffering of I/Os and supporting different voltage levels with the help of cadence tool, Incisive Simulator v (NC-SIM)*

**Keywords** — *high speed I/O, bidirectionality of I/Os, buffering of I/Os, cadence, Incisive Simulator*

**Introduction:** Basic Input/output System functions

- Communicate between chip and external world
- Drive large capacitance off chip
- Operate at compatible voltage levels
- Provide adequate bandwidth
- Limit slew rates to control di/dt noise
- Protect chip against electrostatic discharge
- Use small number of pins (low cost)

**TOOL USED**: cadence Incisive Simulator

Incisive is a suite of tools from Cadence Design Systems related to the design and verification of ASICs, SoCs, and FPGAs. Incisive is commonly referred to by the name NCSim in reference to the core simulation engine. In the late 1990s, the tool suite was known as ldv (logic design and verification).
Key Benefits

- Fuels testbench automation, analysis, and reuse for increased productivity
- Ensures verification quality by tracking industry-standard coverage metrics
- Drives and guides verification with an automatically back-annotated and executable verification plan

**Need for high speed I/O:**

- High speed I/O circuits are becoming increasingly critical as technology scales to increase system bandwidth and decrease power dissipation, die area and system cost.
- The per-pin bandwidth is scaling with device speed at approximately 20% per year.
- High speed I/Os use incident wave signaling wherein a signal is detected on its first traversal of the signal line and absorbed by a receive termination.
- This basically enables the data bandwidth to scale with transistor performance, independent of the line-length. At high data rates, several data bits may be in transit at once – pipelined along the length of the line.
- Traditional I/O designs (e.g. LVCMOS) have a bandwidth that is limited by the by the length of the signal line rather than transistor performance. Their data bandwidth is tied to the length of the line, independent of transistor performance, resulting in a bottleneck as bandwidth demands increase.
- More than half of the power dissipation of many systems today is I/O power, and steadily the fraction of I/O power is increasing.
- The minimum current required per I/O is nearly constant, independent of bit-rate; thus high speed I/Os give more bandwidth for this fixed power. Thus, a better process technology not only enables a higher bandwidth per channel but also reduces the energy consumed per bit

**Key Parameters of any I/O:**

- Technology/Fabrication
- Number of pins
- Voltage levels
- Current thresholds
- Clock speed
- Latency
- Power
- Temperature
- Noise margin
- BER
- Jitters at high speeds
- Slew rate control
- Cross talk
- Skin effect
- Multiple families
- Synchronization
- Boundary scan for testing
- Programmability
- RF issues (high frequency)
- Pitch – distance between any 2 pins of an IC
- Variable & multiple programmable Pull up/ Pull Down

**High speed IO Design challenges**

- Types of Logic family specifications & how they are implemented
- Techniques for high speed & very high speed I/O on FPGA
- I/O – key performance parameters

- Implementing Multiple Logic families on Single I/O PAD or pin
- I/O Specifications are normally Analog, but we have to implement & achieve Digital Functionality
- Hot swap of logic levels - switching to different logic levels without switching the process
- Implementing & achieving GPIO & SPIO is very complex process
- Implementing high speed PIN TRANSCEIVER is very difficult
- Implementing & auto Switching of variable & programmable pull up & pull downs

### Proposed Methodology

In line with the latest high speed I/O trends & functionalities & also keeping in mind the best strategy to address maximum number of previously listed open issues, the top-level architecture for the proposed Next Generation High speed I/O is as shown in the figure.

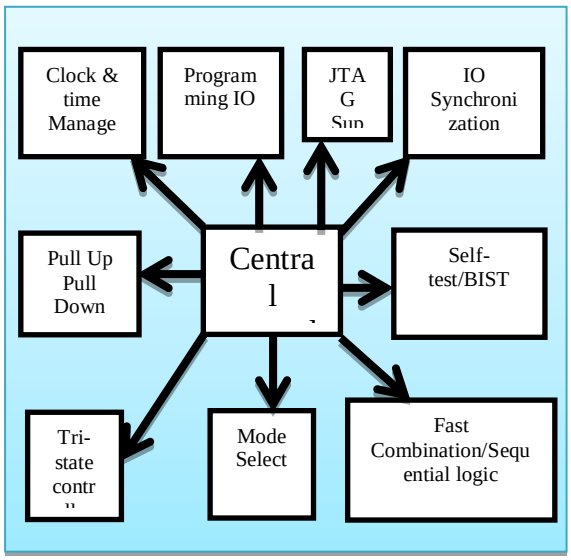


*Fig 1: Proposed High speed programmable I/O*

## RESEARCH DESIGN

### *A. Module 1: Bidirectional I/O*

As can be seen in the below figure, a bi-directional IO control Digital circuit is designed using 2 tri-state buffers & 1 inverter

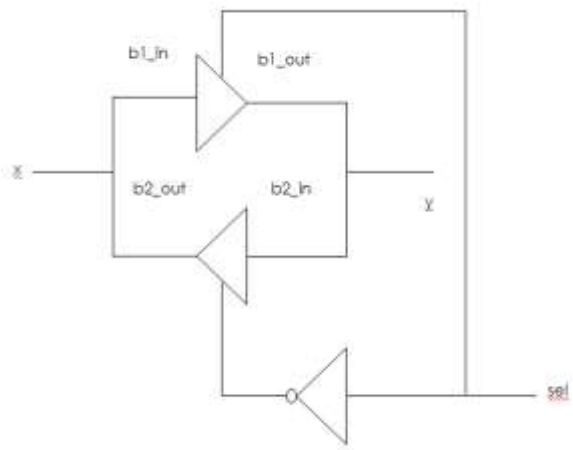


*Fig 2: Bidirectional I/O*

| Select input | input | output | Signal direction |
|---|---|---|---|
| 0 | X | Y | X to Y |
| 1 | Y | X | Y to X |

The table explains the working of the bi-directional with select line control input the signal flow direction:

1. When select signal sel=0, buffer 1 (b1) is enabled & Y=X, buffer 2 [b2] is disabled & hence b2_out tri-stated, X becomes input & Y acts output [signal flow is from X to Y]
2. When select signal sel=1 buffer 2 [b2] is enabled & X=Y, & buffer 1 (b1) is disabled &hence b1_out is tri-stated, Y becomes input & X acts output [signal flow is from Y to X]
3. Since multiple driver errors occur during simulation of any bi-directional logic or signal, the two signal direction situations are simulated separately, as indicated in case 1 & case 2 respectively.

Case 1: X as input & Y as output, signal flow from X to Y

As can be seen in the simulation waveform:

1. Select signal is toggled alternatively between 0 & 1.
2. Whenever sel=1, Y gets the value of X i.e., X becomes input & Y becomes output & hence data or signal flows from X to Y.
3. When sel=0, Y is tri-stated in simulated, but when the design is implemented on FPGA, signal flows from Y to X

*Fig 3: X as input & Y as output*

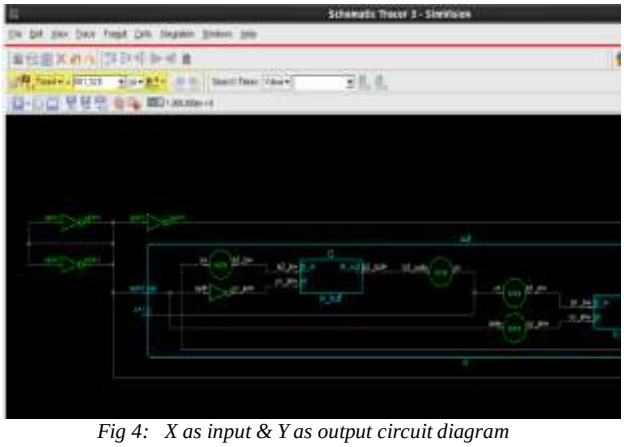

*Fig 4: X as input & Y as output circuit diagram*

Case 2: Y as input & X as output, signal flow from Y to X

As can be seen in the simulation waveform:

1. Select signal is toggled alternatively between 0 & 1.
2. Whenever sel=1, X gets the value of Y i.e., Y becomes input & X becomes output & hence data or signal flows from Y to X.
3. When sel=0, Y is tri-stated in simulated, but when the design is implemented on FPGA, signal flows from Y to X

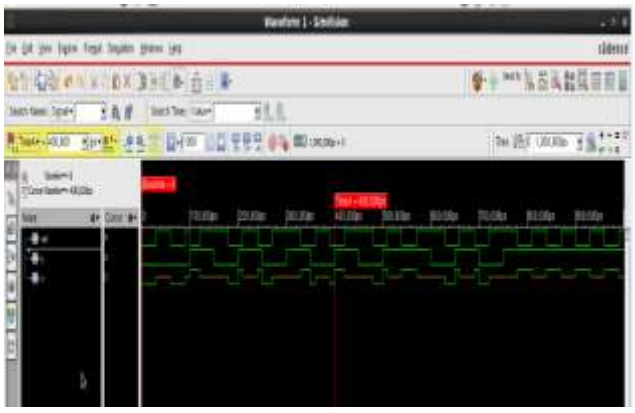

*Fig 5:* Y as input & X as output

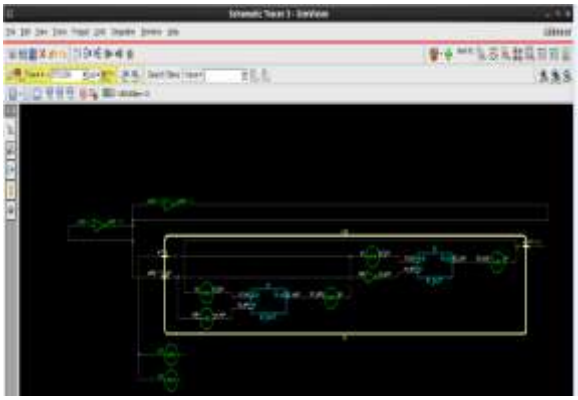

*Fig 6:* Y as input & X as output circuit

### *A. Module 2: Programmable select I/O*

In the below figure, a Digital design to implement programmable select IO [for any Input pins] is shown

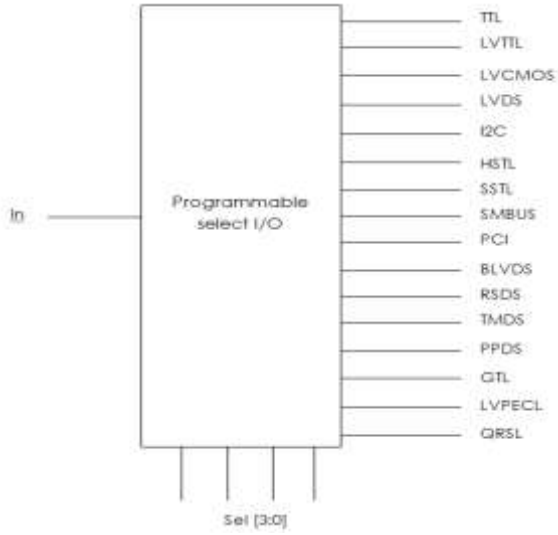


*Fig 7: Programmable select I/O*

| PC [3:0] | Input or Output signal routed to |
|---|---|
| 0000 | TTL |
| 0001 | LVTTL |
| 0010 | LVCMOS |
| 0011 | LVDS |
| 0100 | I2C |
| 0101 | HSTL |
| 0110 | SSTL |
| 0111 | SMBUS |

| | |
|---|---|
| 1000 | PCI |
| 1001 | BLVDS |
| 1010 | RSDS |
| 1011 | TMDS |
| 1100 | PPDS |
| 1101 | GTL |
| 1110 | LVPECL |
| 1111 | QRSL |

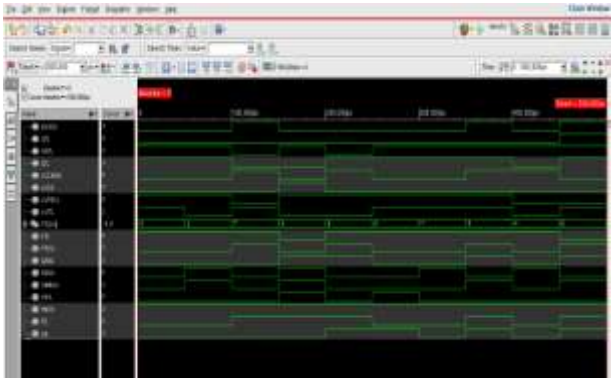

*Fig 8: Simulation waveform of Programmable select I/O*

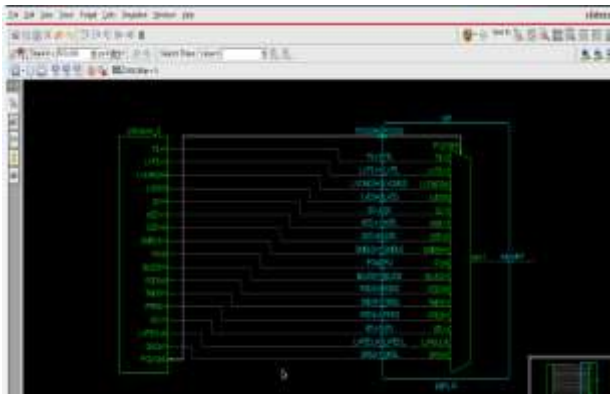

*Fig 9: circuit of programmable select I/O*

In the above figure 8, a Digital design to implement programmable select IO [for any output pins] is shown. Here, the output signal from inside FPGA is routed through any of the 16 pre-defined Digital logic family to any IO bank, depending on the programmable control inputs - PC [3:0] as shown in the table above. The output pin will exhibit such characteristics of the particular digital logic families according to the power bank [fan-in & fan-out will be enabled automatically]

### *B. Module 3 Bidirectional functionality with buffering*

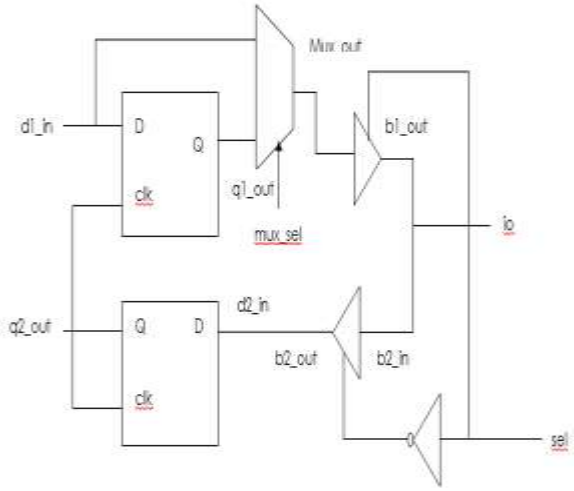


*Fig 10: Bi directional functionality with buffering*

As can be seen from the above simulation waveform, clock is free running at any suitable frequency.
When sel=0, non-buffered d1_in comes out at b1_out. B2_out & d2_out are tri-stated.
When sel=1, d1_in is buffered through input buffer flip-flop & comes out as q1_out, which in turn gets applied to mux & comes out of multiplexer as mux_out=q1_out
Whenever b1_en=1, io=b1_out=d1_in [non-buffered when sel=0] &io = b1_out=q1_out=delayed d1_in [buffered when sel=1.

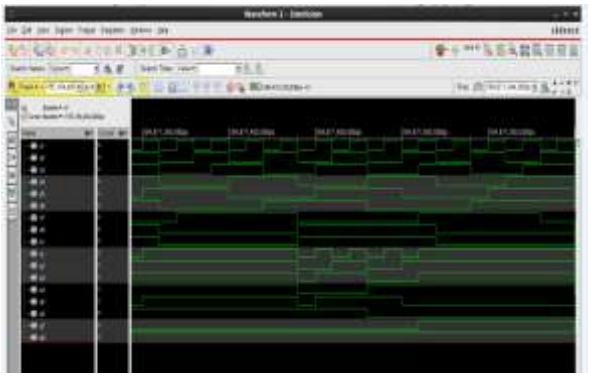

*Fig 11: Simulation waveform of Bi directional functionality with buffering*

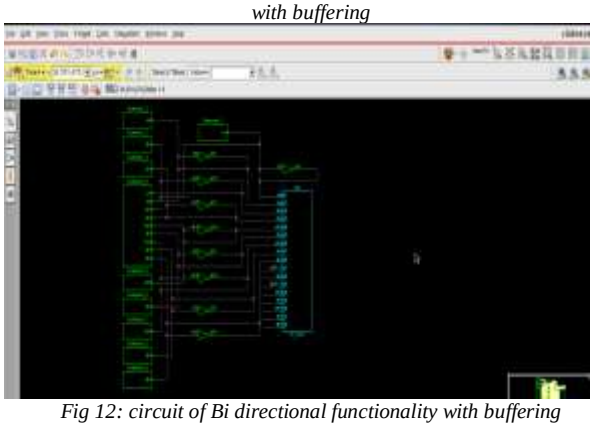

*Fig 12: circuit of Bi directional functionality with buffering*

**Power summary:**

| Module | Cells | Leakage Power(nW) | Dynamic Power(nW) | Total Power(nW) |
|---|---|---|---|---|
| io _buffer | 6 | 1.314 | 1572.917 | 1574.231 |
| io | 2 | 0.367 | 580.437 | 580.804 |
| pgm_io | 22 | 7.215 | 12855.195 | 12862.41 |

## CONCLUSION

Aligned to the key findings helped me to explore & understand the various types of I/Os used in contemporary processors, memory, ASSPs, FPGA etc., their features & functionalities. With all these knowledges, I am able to design and simulate the I/O functionalities like - Bidirectional I/O, Programmable select I/O, I/O with Bi directional functionality & buffering using cadence tool. Results of each module is indicated & explained along with micro level digital design. All these functionalities implemented along with a few more proposed modules put together will be aimed towards the prototype development of Next generation programmable High Speed I/O.

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