A Review on ASIC Flow Employing EDA Tools by Synopsys

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Abstract

The development in automation tools and their algorithms has made it convenient to design ASIC processors and perform extensive analysis of their parameters. Application Specific Integrated Circuit (ASIC) design flow provides the flexibility of modeling the blocks as hardware accelerator which can be made a part of the chip. In ASIC flow there are various processes like logic or physical synthesis, static timing analysis, formal verification, design for testability which provides details about area, power, timing information, violating paths that required for designing the block to so that it can be integrated into the chip along with other blocks. In regard to this, the paper provides an insight to the brief literature survey of the proposed works, their functioning with respect to Synopsys's EDA tools and the dependency between these tools. Thus, the methods used in the flow are designed such that the critical parameters of the design like power, area and timing can be optimized to a great extent with the aid of EDA tools.

Keywords - *Application Specific Integrated Circuit, Register Transfer Logic, Electronic Design Automation, Design Compiler, Prime Time, IC Compiler, Synthesis, Timing Analysis, Floor planning, Optimization, Power, Area.*

I. INTRODUCTION

With the growth in technology and design automation, it has become possible to interrelate hardware and software aspects of the design. Electronic design automation (EDA) refers to the collection of software tools and algorithms used for designing electronic systems (hardware blocks like ICs and PCBs). Digital design flow is a fully automated process and consists of steps that requires tool set at each step of the process. So, FPGA and ASIC projects require a complete set of computer aided design tools. EDA tools interconnects hardware and software design as shown in Figure 1 in terms of correctness, productivity, optimality and scalability as it is known that steps involved in ASIC design are expressing the functionality by writing in RTL code in Verilog/System Verilog, synthesizing Verilog code into a netlist of technology dependent cells which is obtained after performing translation, mapping and optimization of RTL code (knows as logic synthesis process) followed by physical design which includes floor planning, placement, clock tree synthesis, routing and optimization (pre and post route optimization) and static timing analysis. STA is followed by formal verification of synthesis process and power estimation techniques.

Each of these stages (synthesis, static timing analysis and floor planning) are complex and most of them are repetitive. With the exponential growth in the number of transistors in a chip from thousands to million to billion, it not humanly possible to perform synthesis, static analysis, floor planning etc. Thus, EDA(Electronic Design Automation) software implements the algorithms necessary for different stages of IC design. EDA tools provided by Synopsys are – Design Compiler for running synthesis flow, prime time for static timing analysis and IC compiler for placement and routing solution.

II. EDA TOOLS PROVIDED BY SYNOPSYS

Design Compiler delivers superior quality of results and organizes the flow for a faster and predictable design implementation. Design Compiler makes use of advanced optimizations techniques combined with accurate net delay modeling to achieve 5% faster timing post-placement with the help of technology libraries, symbol libraries and Design Ware libraries. Design Compiler further provides DC Ultra topographical technology to provide physical support to IC Compiler tool, helps in tightening timing and area correlation between synthesis process and placement process up to 5% while aids in speeding-up IC Compiler placement process by 1.5 times. The main features of Design Compiler tool are to provide advanced optimizations, generation of QoR at faster rate and translation of designs from one technology to another happens quickly [1-3].

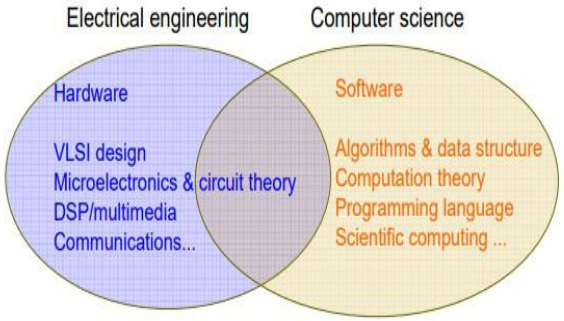

Fig 1: Interaction between Software and Hardware with the help of Electronic DesignAutomation

Prime Time is a tool provided by Synopsys to carry out static timing analysis. This tool provides trusted signoff solution for timing, signal integrity and power analysis for any top-level design. The tool delivers accurate signoff information which helps in overcoming the shortcomings thereby reducing the risk and cost of the design. Used for both small and large designs, prime time tool provides great productivity and silicon success through high accuracy and predictability. With this tool, checking for setup and hold time, clock gating constraints, minimum period and minimum pulse width for clocks and design rules including maximum/minimum transition time, capacitance and fanout is performed. Figure 2 and Figure 3 show the pre layout design and post layout design for ASIC flow respectively. The flow includes various stages of ASIC flow like logic synthesis, static timing analysis and floor planning on which various constraints are applied [5].

IC compiler tool is used in placement and routing and aims at delivering best quality of reports for all the designs across various technologies. This tool includes features like flat and hierarchical design planning, early design exploration, congestion-based placement and optimization, clock tree synthesis and signoff closure. This tool has been architected for providing great power, performance and area along with parallel optimization processes like – global placement, routing driven placement optimization, clock and data optimization, total power optimization, machine learning driven optimizations [6]. Prime Time delay calculation with IC Compiler gives place and route QoR with greater design convergence. Figure 4 shows the design platform making use of various EDA tools of Synopsys company. Prime Time tool is used both with Design Compiler and IC Compiler as there is a need of accurate timing analysis post synthesis and Floorplanning in ASIC design flow.

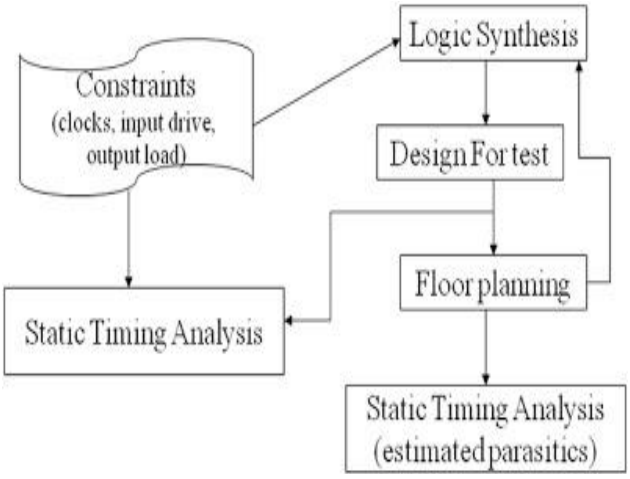

Fig 2: Pre-Layout Design of ASIC flow

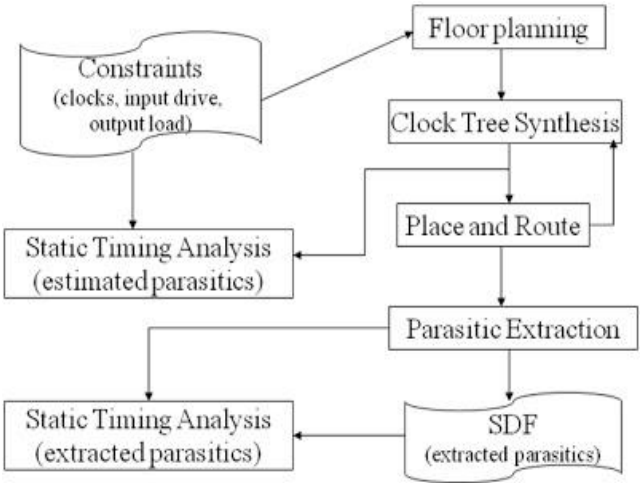

Fig 3: Post-Layout Design of ASIC flow

Fig 4: Interrelation between different EDA tools provided by Synopsys

III. LITERATURE SURVEY

The different types of methodologies carried out in synthesis flow with the help of Design Compiler tool, in timing analysis with the help of PrimeTime tool and in floor planning with the help of IC Compiler tool is available in the literature. The main aim of all the proposed work is to improve the efficiency of the design flow and to optimize the three important parameters – power, timing and area significantly.

In paper [1] comparative study of area, power and timing results of the case study is presented by performing scan insertion synthesis and synthesis with and without constraints. With suitable inbuilt optimization and mapping techniques, Design Compiler performs synthesis and optimization and Conformal EC tool performs Logic Equivalence Check (LEC) on the case study.

In paper [2] a technique for enhancing area, power and performance by applying an ungrouping method in synthesis stage of Design Compiler tool and an optimization method in floorplan, placement and clock tree synthesis of IC Compiler tool is proposed. The comparative analysis of results of concurrent clock and data optimization and conventional clock tree synthesis implies that with concurrent clock and data optimization technique area, power (static and dynamic), worst negative slack and total negative slack is improved. Therefore, the Synopsys tools work efficiently in improving the overall behavior of the design.

Paper [3] presents a synthesis technique using Synopsys Design Compiler involving a combination of PTL and CMOS logic cells, which can be inserted into standard cell-based design flow. The experiments based on UMC 90-nm technology conveyed that PTL surpasses CMOS in terms of parameters like power consumption, area, and area–delay–power product while hybrid CMOS/PTL yields better results in area-optimization and delay optimization-based synthesis flow. Therefore, PTL and hybrid CMOS/PTL can be employed in applications having delay, power and area as critical parameters in the design.

Paper [4] focuses on power reduction in scan synthesis stage of automatic test pattern generator. The aim of reducing cell internal power, net switching power and total dynamic power by 50% is achieved by applying low power techniques to phase locked loop circuit with the aid of Synopsys Design Compiler tool. Another important inference that can be drawn is that scan clock frequency reduction has impact only on power and not on IC's functionality and performance. Thus, Synopsys DC tool plays a crucial in design for testability stage.

In paper [5] a tool - Primetime Timing Report Web-based Analyzer is presented which is used to perform tasks such as analysis of timing report for various design stages, clock skew analysis and computation of path constraints for timing debugging. All the results are displayed in PHP based website which makes it very easy to access them. Thus, PTWRA tool is a way to generate accurate timing reports as in very application timing is becoming a critical factor which needs to be considered for obtaining efficient implementation of designs.

In paper [6] Genus Synthesis tool by Cadence in synthesis process, Synopsys IC Compiler tool in placement and routing and Tempus tool in sign-off static timing analysis is employed. VSDFLOW is tested on designs like picorv32 - a RISC-V CPU core which makes use of 180nm PDK's and 45nm PDK's from OSU and Nangate respectively and comparison drawn based on the results of different combination of tools by running VSDFLOW multiple times shows that with each design, the area is optimized.

Paper [7] puts forward a methodology of performing timing analysis which is aware of negative bias temperature instability (NBTI) and hot carrier injection (HCI) ageing effects. In the traditional methods, these ageing effects were not a part of design, so the proposed methods are designed in such a way that the design flow methodology takes care of these ageing effects which is accomplished by combining "ageing analysis" with static timing analysis tools – PrimeTime. Thus, the flexibility of Eda tool enables ageing models to be included in the flow and the other feature offered by PrimeTime is that its already existing features can be used in accordance to ageing model. Therefore, the development of ageing model and its combined functioning with STA tool enables to reduce some of the other effects like Time Dependent Dielectric Breakdown (TDDB) as well.

In paper [8] a 3-D design automation flow for integrated circuits enables to perform to static timing analysis using PrimeTime tool and power estimation using PrimeTime PX tool is proposed. The 3-D integration methodology is designed such that it provides 14.6% of average power reduction, 18.7% of performance improvement, 49% reduction of footprints, 10% decrease in power and 11.6% decrease in peak power in comparison to 2-D design integration procedure. Therefore, the comparative analysis convey that 3-D integration method is more efficient in terms of providing required optimal values of critical parameters and can be used for any real time application involving design of ICs.

In paper [9] a technique of design flow using multiple threshold cells with 16nm FinFET technology with implementation being carried out using tools like Innovus, IC Compiler II and Calibre Design RVE is put forward. The proposed work aims improving the power consumption as this parameter directly affects the performance and lifetime of the chip. Also, power gating techniques are applied to overcome the issue of high-power consumption at nanometer technologies. The results showed that with power switches being inserted in the design, the switching power got reduced by 26.77% and total dynamic power consumption was reduced by a factor of 35.32%. The multi threshold cells helped in reducing leakage power by 80.79%. Therefore, this proposed work mainly aims at reducing different types of power for any design and hence this technique can be used in the applications where power (either leakage, switching or dynamic) is a critical parameter.

Paper [10] presents an algorithm for characterization of non-3-D monotonic cells to fit in 3-D monotonic setup as this leads to PPA boasting. It is seen that by selecting 3-D monotonic cells from standard library, PrimeTime tools provides excellent PPA gain. Therefore, PPA gain is an important factor in any design as it offers advantages with respect to size of CPU and performance enhancement. Hence, the main aim of the proposed work is to establish relation between ASIC tool cost function and STD cell library files (.lib file).

IV. METHODOLOGY

In all the real time applications, ASIC flow is extensively used for modelling any block as a hardware accelerator which is possible with the help of a range of EDA tools. The modelling of a block as a hardware to be implemented in a chip, begins with writing its Verilog code. The Verilog code along with other inputs files undergoes logic synthesis where in the syntax of RTL code is checked and three main steps are carried out – translation, mapping and optimization using DC tool. The synthesized netlist then undergoes static timing analysis to check for accuracy of timing paths and reduction in number of violating paths using PrimeTime tool. The synthesized and optimized netlist with post timing signoff values undergoes placement and routing where in the design is partitioned, placed and routed as per the physical requirements of the design using IC Compiler tool and again timing analysis is done to check if the placement and routing activity (P&R) has brought in any changes in the timing performance of the design. Post clean timing signoff, output files are generated.

Design Compiler tool of version - 2019.03-SP5 is used for performing synthesis flow, PrimeTime tool of version - 2018.06-SP5 is used for performing static timing analysis and IC Compiler tool of version 2016.03-SP4 is used for performing placement and routing. Constraints are applied to the input files and these tools help in assessing the constraints and their effect on the results. Constraints which includes design and optimization constraints are the main driving factor to obtain the particular results. The tools aim to meet both (Design Rule Constraints (DRC)) and optimization constraints with DRC having higher precedence over optimization constraints. These constraints define the behavior and functioning of a particular block. Every block being designed for a chip has a set of constraints which are necessary to be satisfied to achieve the desired working of the block.

Design Compiler tool performs synthesis on the design and based on the applied constraints, it generates the synthesized and optimized netlist design which is the made up of standard library cells (ASIC library). The reports of synthesis flow convey the details about area, power and timing values. There are chances that timing values changes or gets affected post synthesis and might not be as per the specifications so here static timing analysis performed by PrimeTime tool plays a crucial role in bringing in the timing values like setup time, hold time, path delays within the threshold levels so that the synthesized netlist is compatible with the user specifications. Once the timing analysis yields appropriate results, placement and routing activity is carried out with the aid of IC Compiler II tool for the synthesized and optimized netlist so that based on this, design becomes ready for fabrication on the silicon chip. So, synthesis flow, timing analysis and placement and routing are three crucial activities performed in ASIC flow design.

V. CONCLUSION

The results of the proposed work have vast applications in the field of VLSI and chip designing and the main objective is to understand the working of each EDA tool of Synopsys and their dependency on each other. From the literature survey, it is evident that all the proposed works convey the working of Design Compiler, PrimeTime and IC Compiler tools and their interrelation and their way of obtaining PPA exploration. The main aim of developing hardware accelerators is their efficiency which makes them a better version of their software counterpart. So, for designing any hardware accelerators it is necessary to know about its crucial parameters like - required area on the chip, power consumption and timing values for slack, skew, delays which in turn impact other interrelated blocks on the chip. Thus, these parameters

can be calculated using logic synthesis methodology with the help of synthesis tools. Designing hardware accelerators to perform the crucial activities is going to bring in a lot of development in the field of VLSI and SoC chip design.

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