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# Review Shop Store Quantum-Dot Cellular Automata

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***Abstract*** — *Quantum-dot Cellular Automata is = = an upcoming futuristic technology that offers key features like high speed, low power consumption, low size, etc., are emerging nanotechnology combined with dynamic and dynamic performance wisdom. In order to test this technology, we propose a model of a logic compilation of QCA circuits. There are many studies reported on it the formation of flexible logical gates compared to the flexible TR. This paper shows the possible formation of rational exible gates of the QCA. QCADesigner is recognized for performance signs and mimics the proposed gates. In the future, these gates could be used for the construction of complex computer structures.*

**Keywords –** *Alternative of CMOS , CMOS, Nanotechnology , QCA , Reversible Logic Gates*

## I. INTRODUCTION

One of the promising methods for nanotechnology is CMOS, CMOS is very popular and widely used, but the future of nanotechnology is QCA. The basic building block for making a QCA unit is the QCA cell. Every QCA cell has four vacant places known as quantum dots, these quantum dots are present on the edge of a cell which is basically a square block, and to these vacant places, only two electrons are free. QCA is based on binary data recording in charging configuration within quantum dot cells. Electron tunneling is used by the two portable electrons to transmit different quantum dots to the QCA cell. Coulombic irritation will cause the charge to enter only the corners of the primary unit of the block leading totwo direct divisions in a cell

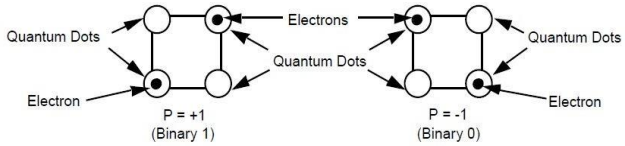


**Figure 1: Polarization of A QCA Cell for different representations**

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Farther than two equilibrium systems with two equal electronsin the QCA cell, indicating cell division P = +1 and cell division P=-1. The Cell division of Positive P represents 1 binary, while the cell division of Negative P represents 0 binary.

### *A. QCA Basic*

The primary attribute of the QCA tool is QCA cell. The basic structural block of a QCA is acell with- four vacant spaces known as quantum dots that are placed in the quarter of a square cell and two free electrons. Build upon the position of these free charges; the basic cell has 2 types of polarization (P). P = Positive (Binary 1) when cells 1 and 3 are active,while charges at sites 2 and 4 lead to P = Negative (Binary 0), as shown in Figure 1.

### *B. Basic QCA Device Multi-Gate Device*

The sound basis of QCA is the 3 input gates from Figure 2. Computer calculation at many gates is made by driving the device cell to its minimum power level. This is happening when considering the separation of multiple input cells from three. We need an input cell just as it is replaced by a widespread signal in the direction of the device cell. The chamber will always take a lot of division because this is a division when it is released; the electronsin the middle of the electrons present in the 3 input cells, and the tool cell will be smaller.

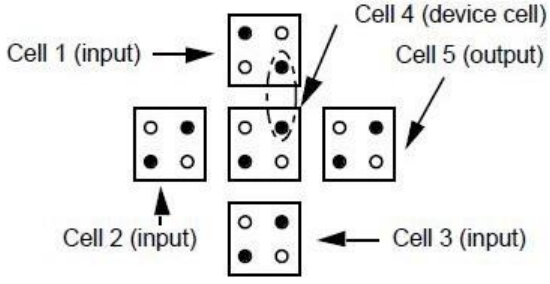


**Figure 2: The basic block of the QCA logical device**

To understand how a tool cell reaches its minimum energy state lets us consider Coulombic cells in alternative cells 1 and 4, and cells 2 and 4, and cells 3 and 4 Coulombic interactions between negative charge in cells 1 and 4 will usually lead to cell 4 changing its appearance; as a result electron reverse. However, cells 2 and 3 also attack the cell division 4 and 1 had a P = + 1 division. As a result, because many cells attack the device cell with the P = + 1 division, it will also look at this division because the Coulombic connection is stronger than P = -1.

### *C. The Basic Clock*

In traditional Very-large-scale integration (VLSI) technologies, the clock process is used to control time sequentially regions. In this nanotechnology, the pipeline-based clock process is vital for successive integration and construction. This method not only controls the flow of data but also empowers cells. For the purpose of setting the clock, 4 clocks are used. All Clocks are 90 clocks outside the category, as shown in Fig. 3. Every clock in QCA contains four categories of clocks. In transition mode, the bock begins to divide and enlarge the barriers among the dots, and the QCA cell goes to one of the dividing regions depending on the driving state of the cell. In this section, The actual calculation is possible. In the middle of the shooting phase, the cells have a f i xed separation to initiate the next phase.

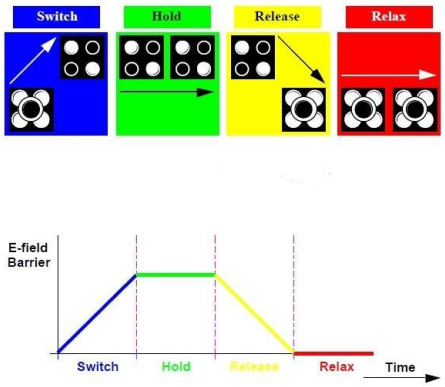


**Figure 3: The four juncture of the QCA clock**

In the liberation phase, the cells began to become political neutralist, and during the final phase, the barriers between the dots are constantly reduced again; the cell has no f i xed partition.

### *D. Reversible Logic Gates*

Reversible gates are used for circuits (gates) with the one-to-one map that differ between inputs vectors and output, so the input value should be equal to the output and also possible to predict the input based on the output and the gate connections. Drawing 4. exhibitions several blocks of the most common and widely used reversible gates. The recyclable logic circuit is widely used in minimizing power consumption, such as low-power building, quantum computing, and computer graphics.

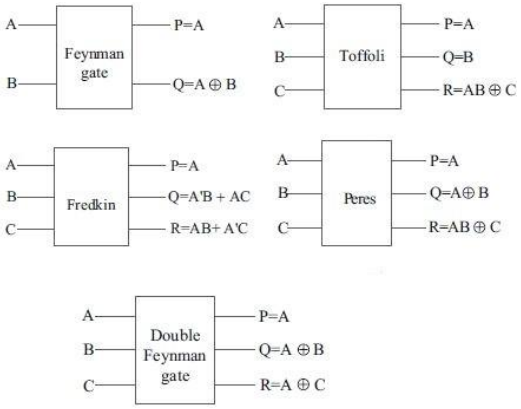


**Figure 4: Commonly used reversible gates.**

## II. Simulation And Results

### *A. Reversible Feynman Gate*

The implementation of Feynman's gate made by QCA blocks is shown in Figure 5 is proposed by many authors. Here, two inputs, i.e., A and B, and two outputs, i.e., X and Y. The logical expression for this region is X = A, Y = AxorB .

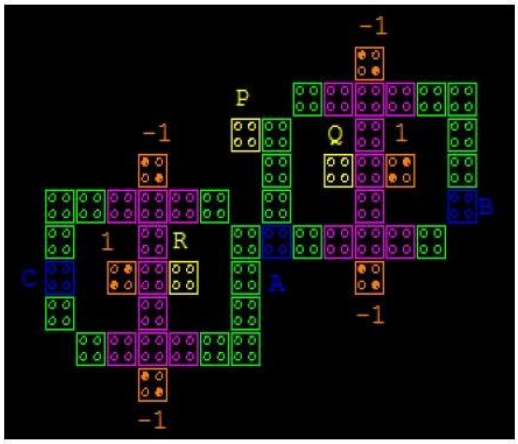


**Figure 6: Double Feynman Gate.**

### *B. Double Feynman Gate*

The QCA petition of this gate is shown in Figure 6 . Here, A, B, and C are the ideas, and theP, Q, and R are the responses for the same. The logic for this place is P = A, Q = AxorBand R = AxorC .

### *C. Tofoli Gate*

The QCA use in the Tofoli's gate is shown in Figure 7. Here, A, B, and C are ideas, andthe results for that are P, Q, and R. The logic for this region is P = A, Q = B, and R = (AB) xorC .

### *D. Fredkin Gate*

QCA application of Fredkin's gate is shown in Figure 8. Here we have three inputs, i.e., A, B, and C, and the results are P, Q, and R. The logic for that place is P = A, Q = A'B + AC,and the value of R = AB + A'C .

### *E. Peres Gate*

QCA application of Peres's gate is shown in the Figure 9. Here, A, B, and C are ideas, andthe results are P, Q, and R . The expression for that is P = A, Q = AxorB and the value ofR = ABxorC .

## III. Results

In this section, the effects of the pretend form of the proposed design are discussed. We have used five basic and standard logical flexible gateway and simulated using a 2.0.3 QCA designer. Circuit performance is verified from the simulated format. The first part of the results describes the simulated waves of the Feynman gate shows in Figure 10 and then the Double Feynman gate in Figure 11 and similar Figure 12for For Tofooli and Figure 13of the gate of Fredkin and in the last Peres gate in figure 14 .

## IV.CONCLUSION

This paper examines the optimal design of Feynman's gate, Double Feyman Gate, Tofoli Gate,peres gate, and Fredkin Gate using a QCA with a minimum number of QCA blocks as a minimum of potential designs. Imitation results indicate that the proposed setup is performing best. During construction, the main focus is on reducing the number of cells and reducing the area. This paper helps to set up a highly sophisticated computer design using flexible gates.

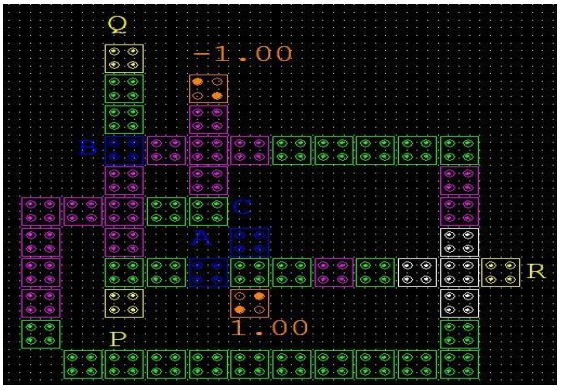


**Figure 7: Tofoli Gate.**

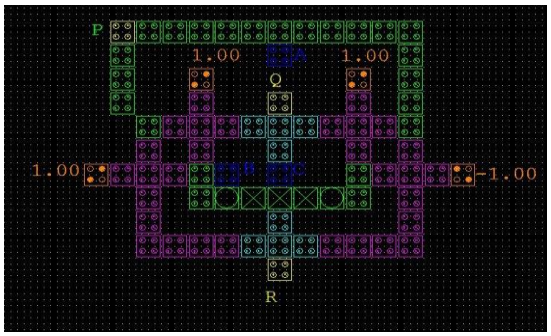


**Figure 8: Fredkin Gate.**

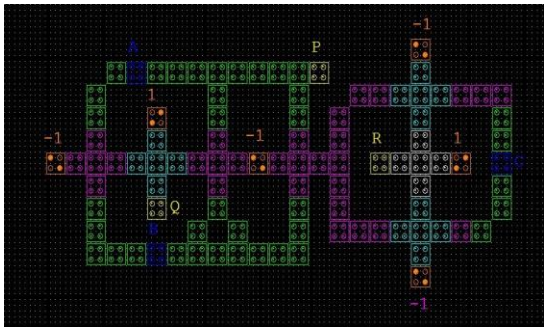


**Figure 9: Peres Gate.**

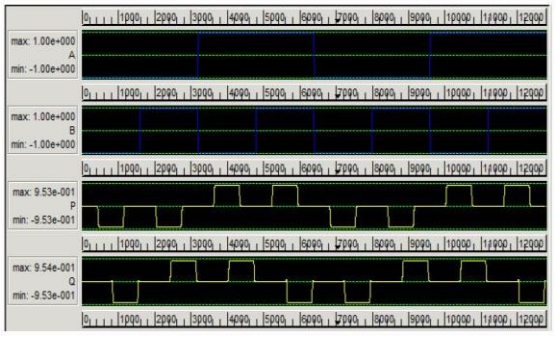


**Figure 10: Imitated Feynman gate simulation form**

**Figure 11: Imitated Double Feynman gate simulation form**

These projects also use techniques like optical computing, quantum computing, and digital signal processing. Therefore, this is concluded that the proposed design should be a promising step towards the goal of high-speed, low-energy design in nanotechnology. Future work could be focused on building an additional circuit and a multiplexor circuit using the Feynman gate.

**Figure 12: Formed measurement form of Tofoli gate.**

**Figure 13: Imitated Fredkin Gate simulation form.**

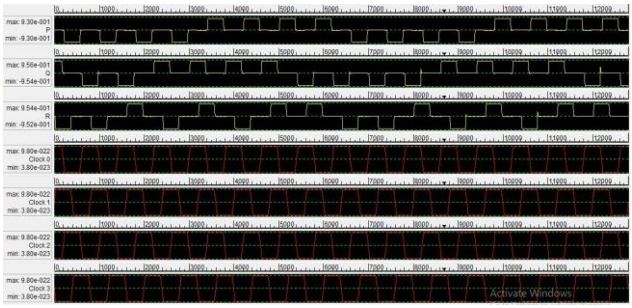

**Figure 14: Simulated waveform for Peres Gate.**

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