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A Novel Coplanar Based XOR/XNOR Structure For Designing QCA Circuits

A. Kartheeswari [1], N.Priya [2], V.Sivani [3], V.Veeralakshmi [4], R.Geeta[5]

[1,2,3,4]*Final year PG Student, AP*[5]
PSR Rengasamy College of Engineering for Women, Sivakasi

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ABSTRACT

Quantum-dot Cellular Automata (QCA) is nanotechnology which is an advance of VLSI research that challenges in contracting CMOS semiconductors mount. In this work, QCA gadgets and utilizations are utilized for those gadgets to fabricate a field-programmable gate array (FPGA). This FPGA has various arrange intelligent squares (CLBs) tiled together. In this work, a novel XOR/XNOR logic with two inputs, two fixed inputs, and one yield is developed. This system is planned in (QCA) nanotechnology for particular engineering configuration utilizing programmable gadgets which provides a minimum area and high performances.

INTRODUCTION

Adders are presented in several structures of microchips square and computerized signal handling. It is a fundamental operation for expansion, deduction, augmentation, and division. Expansion or addition is the combinational circuit that performs expansion of two inputs is known as a Half Adder. And the addition performs with three inputs is known as a Full Adder.

In this paper, a full adder is presented with a base fault rate contrasted and the typical full adder. Using the full adder, the xor/xnor is structured with an advanced system.

II. BASIC ELEMENTS OF QCA

This section discusses the CMOS-VLSI gates that are implemented in QCA. It is based on the principle of Coulomb cooperation between cells. It is adequate to attain the QCA exhibits; consequently, no interconnect wires are required between cells. The fundamental components are the QCA cell, Majority gates (MG), and Invertor. In figure 1, the QCA cell represented that has four quantum dots with two free electrons. The e electrons decide the twofold states that are given in Fig.1

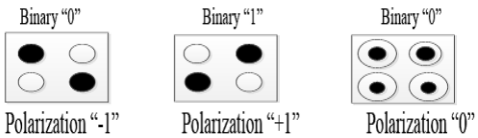

Figure 1: QCA Cell Polarization.

The Neighborhood QCA cells are to be settled in the ground state controlled by the present input status. It is clear that the QCA wire which is used for the cell polarization which is connected the appeared in Figure 2.

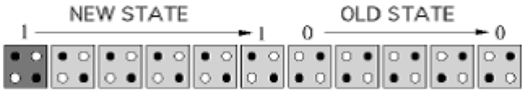

Figure 2: QCA wire

The MG and inverter have appeared in Fig. 3 and Fig. 4, where the MG is the key QCA. The output cell will captivate the cell polarization. The main MG has a three-input logic as A, B, and C that is termed as

$$m(A, B, C) = A \cdot B + B \cdot C + A \cdot$$

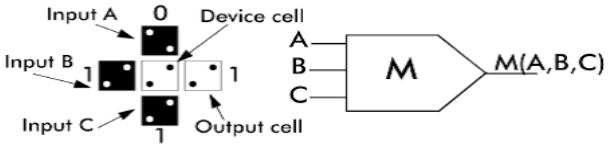

Figure 3: A QCA majority gate

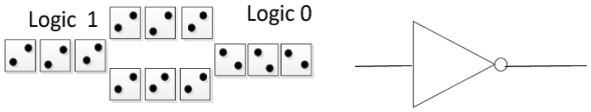

Figure 4: Invertor

With the polarization of "1" or "0", we can get an OR gate and an AND gate individually. Then it can be able to be developed from OR/AND logic gate.

III. PROPOSED SYSTEM

In this section, the novel XOR/XNOR Design is presented. This work presented the XOR/XNOR gates that depend on cell level strategy, and the normal yield would be accomplished by cell impact to one another. It exhibits the novel XOR/XNOR than past XOR/XNOR plans, and the proposed system is not MG and inverter-based. The proposed QCA based circuit of XOR/XNOR is given in Fig. As demonstrated in Fig. 2(a), an and b address input cells, e address empower input cells, while f is yield cell. The design of XOR/XNOR is in Fig 5 that comprises 12

QCA ordinary cells. If the polarization of empowering inputs is '- 1+1', it performs XOR gate. The QCA design of XOR is portrayed in Fig.5.

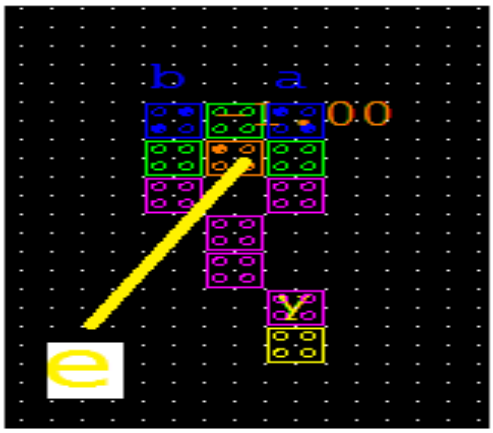

Figure 5: Proposed configurable cell

Proposed full adder

The proposed Coplanar hybrid system that appropriately adjusted normal QCA cells and 45° pivoted cells that don't interface with one another could be utilized. The proposed circuits could effectively involve an inverter and an MG., the least number of gates, are liked to limit the QCA cell. Let the three FA are A0, B0, and Ci, and their outputs are Sum and Carry. The FA is inferred according to conditions (2),(3), and(4). Finally, determining conditions addressing the total and FA output are surrendered (5),(6), and (7).

$$Sum = A_0{}' B_0{}' C_0 + A_0 B_0 C_0{}' + A_0 B_0 C_0 + A_0 B_0{}' C_0{}' \quad (2)$$

$$Sum = A_0{}'\left(B_0{}' C_0 + B_0 C_0{}'\right) + A_0\left(B_0 C_0 + B_0{}' C_0{}'\right) \quad (3)$$

$$Sum = A_0{}'\left(B_0 \oplus C_0\right) + A\left(B_0 \oplus C_0\right)' \quad (4)$$

$$Sum = A_0 \oplus B_0 \oplus C_0 \quad (5)$$

$$C_{out} = MV\left(A_0, B_0, C_0\right) \quad (6)$$

$$C_{out} = \left(A_0 B_0\right) + \left(B_0 C_0\right) + \left(C_0 A_0\right) \quad (7)$$

It requires the QCA cells with two clock stages which are not accomplished in the previous model. The proposed FA is about 0.009µm2 design execution. This plan accomplishes the most minimal dormancy inferable from the less tally of QCA cells.

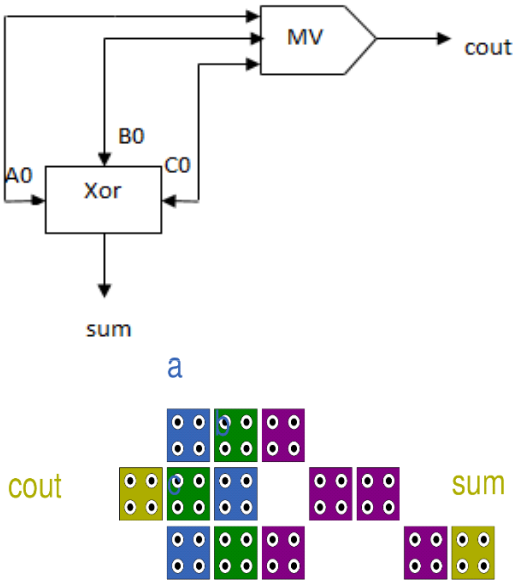

Figure 5(a): Schematic diagram of 1-bit Full adder
Figure 5(b): 1-bit Full adder

IV. RESULTS AND DISCUSSION

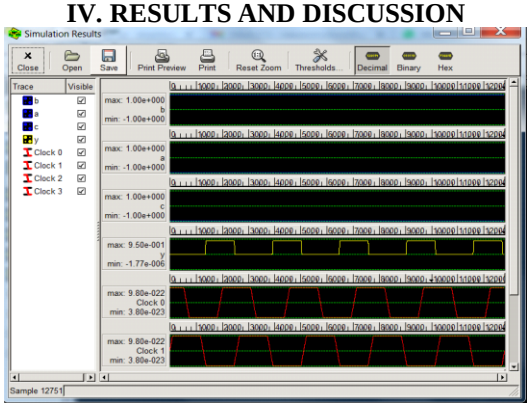

Figure 6: Input Sequence & Output Sequence of configurable cell

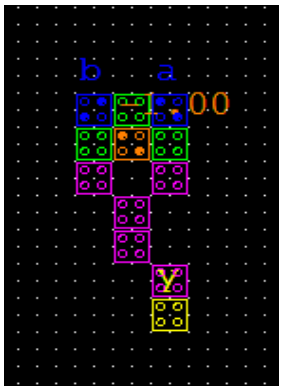

Figure 7: QCA Layout of configurable cell

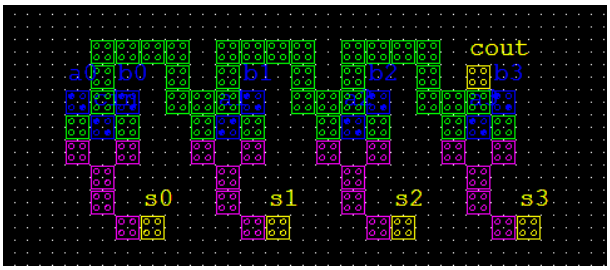

Figure 8: Proposed 4-bit cell

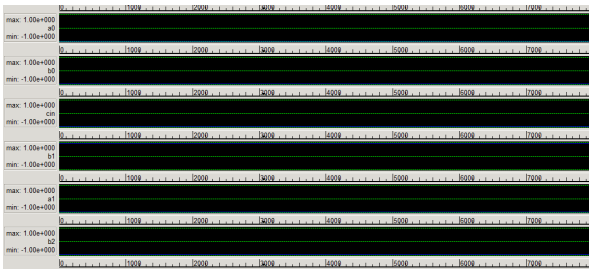

Figure 9: Input sequence

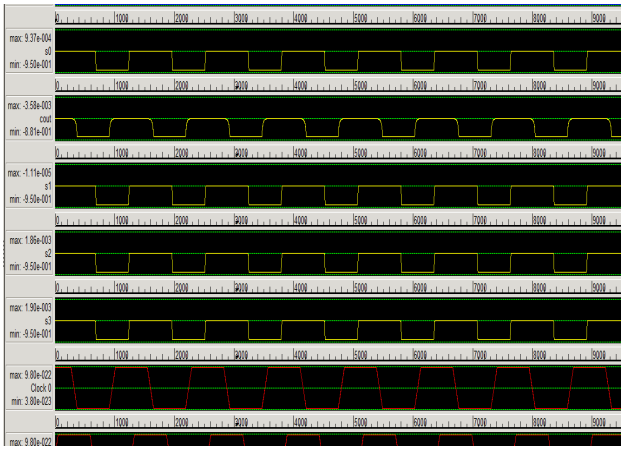

Figure 10: output sequence

V. CONCLUSION

In this work, a novel XOR/XNOR logic with two inputs, two fixed inputs, and one yield is developed. This system is planned in (QCA) nanotechnology for particular engineering configuration utilizing programmable gadgets which provides a minimum area and high performances. The proposed XOR/XNOR has fewer QCA cells and configuration is 0.01, which is the most minimal in general expense.

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