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Original Article

A Novelty of Emergent Technology Challenges of Dielectric Films at 14nm Era

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Abstract *- This paper deals with the challenges ahead of dielectric film applicable in sub-nanometer technology, which will be varying characteristics with different applied methods. To form finfets in the sub-nanometer era. It gets harder for ordinary Field Effect Transistors to compress short-term channel output as technology advances beyond 14nm. For the coming generation, FinFET technology offers a possible solution to those problems. The sophisticated electrostatic controller provided by the FinFET gate wraps channel without significant doping enables reliable distribution and enhanced performance for the CMOS circuit. FinFET can be implemented using a sizable portion of CMOS-based processes. However, many new applications are still available, and difficulties and techniques must be improved to meet the demanding FinFET specifications.*

This study will describe various novel 14nm FinFET dielectric film techniques and applications, including Atomic Layer Deposition boron and phosphor silicate glass solid-state doping, flowable chemical vapour deposition streaming film Shallow-Trench-Isolation (STI), and interlayer dielectric gap fill(ILD), self-portrait films of nitride (SAC), and others. Additionally, the results of those procedures' initial tests will be discussed. The difficulties with those apps will then be thoroughly explained. The issues will be addressed to meet the practical requirements by taking into account the development processes of those dielectric films utilised in various applications.

Keywords *- FinFET, PTSL, BSG, PSG, SCE, CVD, ILD, SAC, STI, Die-electric.*

1. Introduction

FinFET is one of the most promising options for addressing typical FET problems, such as short-term effects and poor electrostatic control brought on by continuous reduction, and more, as technology advances to 14nm and beyond. finFET design is compatible with a substantial portion of conventional CMOS processes, but because of the 3D characteristics of Fins, the process is exceedingly complicated and demands rigorous process control. As a result, several novel techniques and applications, such as dielectric films like Boron and phosphorous SSD films and Flowabl chemical vapour deposition Shallow-Trench-Isolation, were launched for the fabrication of fins and self-alignment contract nitride films, ILD gap fill, etc. Those procedures in the clothes wafer and wafer ware's preliminary test results are exhibited, and prospective issues and advancements are explored. Nano-scale CMOS technology will use multiple channel MOSFET structures like FINFET [1], [2] because they have good gate controllability on channel charge. Air-gap features for crucial layers were patterned on 32 and 22nm node vehicles using traditional 193 nm dry lithography [14]. The 14nm ntel finfet in bulk [3] has a fin-pitch scale (42nm), solid-source sub-fin doping, a double-aligned pattern, and an air gap in the beol. The wings also have a straight edge and a low doping shape. The bottom-oxidation-through-sti (bots) method [4] can produce local flares in oxide for greater fragmentation.

2. Nalysis of Experimentation

2.1. ALD Boron Silicate Glass /Phosphorous Silicate Glass FOR SOLID STATE DOPING

Due to improved heat dissipation and cheaper production costs, a few fins have garnered greater attention than Silicon-On-Insulator (SOI) fins [5]. However, when the channels are smaller, it has a problem with lower channel leakage. To account for leakage, developing an unpunched stop layer (PTSL) employing doping in the sub-fin is considered a potential strategy [6]. Due to Si's concerns about damage, the effects of shadows on Fin, height increases, and other factors, normal doping implantation is constrained. Intel presented the Solid State Doping (SSD) sub-fin for the first time at the 2014 IEDM to improve the punch-through stopper dopant setup [7]. Fig. 1 depicts the streamlined integration procedures for SSD doping. The Boron dopant profile after the Fin depth is shown in Figure 2.

Boron concentrations in BSG films increase to 5E20 atoms / cm^3, comparable to standard basic implants, whereas dopant concentrations reach about 1E19 atoms /

cm^3 on average. The impact of PTSL dopant on the Fin device is lessened since SSD doping is more likely to occur in the dopant profile. This paper also addressed the behaviour of boron (B) and phosphorus (P) dispersion in silicon substrates. The following tests are run on Si garment wafers:

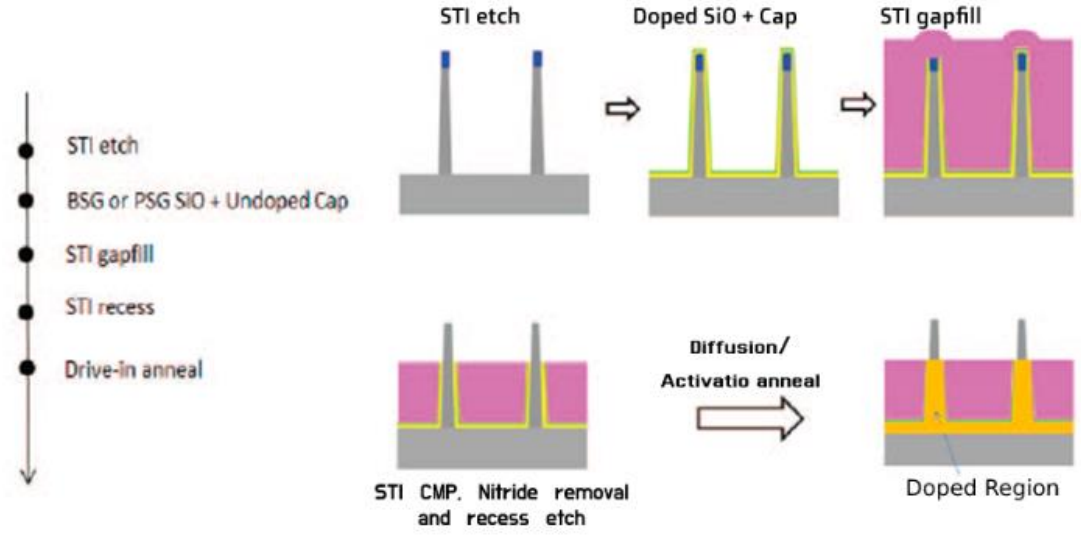

Fig. 1 Steps for solid-state doping simplified

Step I: Using ASM XP8 ALD, 30 Boran silicate GLASS films with a Boran concentration of 6E20at/cm^3 and 30 Phosphorous silicate glass films with a Phosphorous concentration of 5.05E20at/cm^3 are put on Si substrates, respectively. The Si-O_2 capping layer is then applied.

Step II: RTA (Rapid Thermal Anneal) samples heated to 1060°C for 10 seconds.

Step III: SIMS rating is carried out to confirm the dispersion of B and P dopants in Silicon substrate.

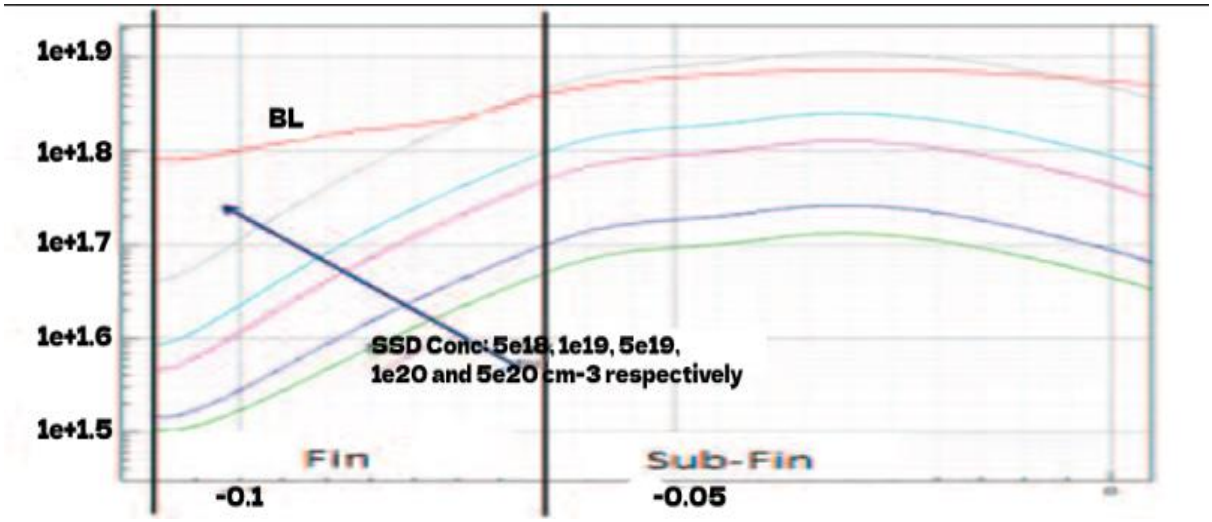

Fig. 2 Profile Boron dopant using TCAD along Fin simulation output

The right-hand arrangement in Fig. 3 (a) represents the concentration of atom B (atoms/cc). The Boron silicate in the BSG layer, located at a depth of 30–60, is scattered after RTA treatment in both the upper SiO2 layer and the Si substrate beneath it, which are located at a depth of 30–5. The Boron signal was outside the acquisition limit (1E * 18) at depths greater than 85, which translates to a 2nm penetration into the Si substrate. Phosphorous dispersion is considerably deeper in the Si substrate than in Boron. 60 to 110 metres deep (as depicted above fig3b.,

Additionally, the slope of the dispersion is uniform. This discovery has revealed the initial active distribution of the B&P dopant. The different distribution behaviour also encourages study by reducing the SIMS method's undesired spraying effect.

The silicon dioxide CAP and Boron-phosphorous silicate glass layers were stripped away, exposing the Si substrate, and the analysis was carried out with a great resolution. The results, which are shown

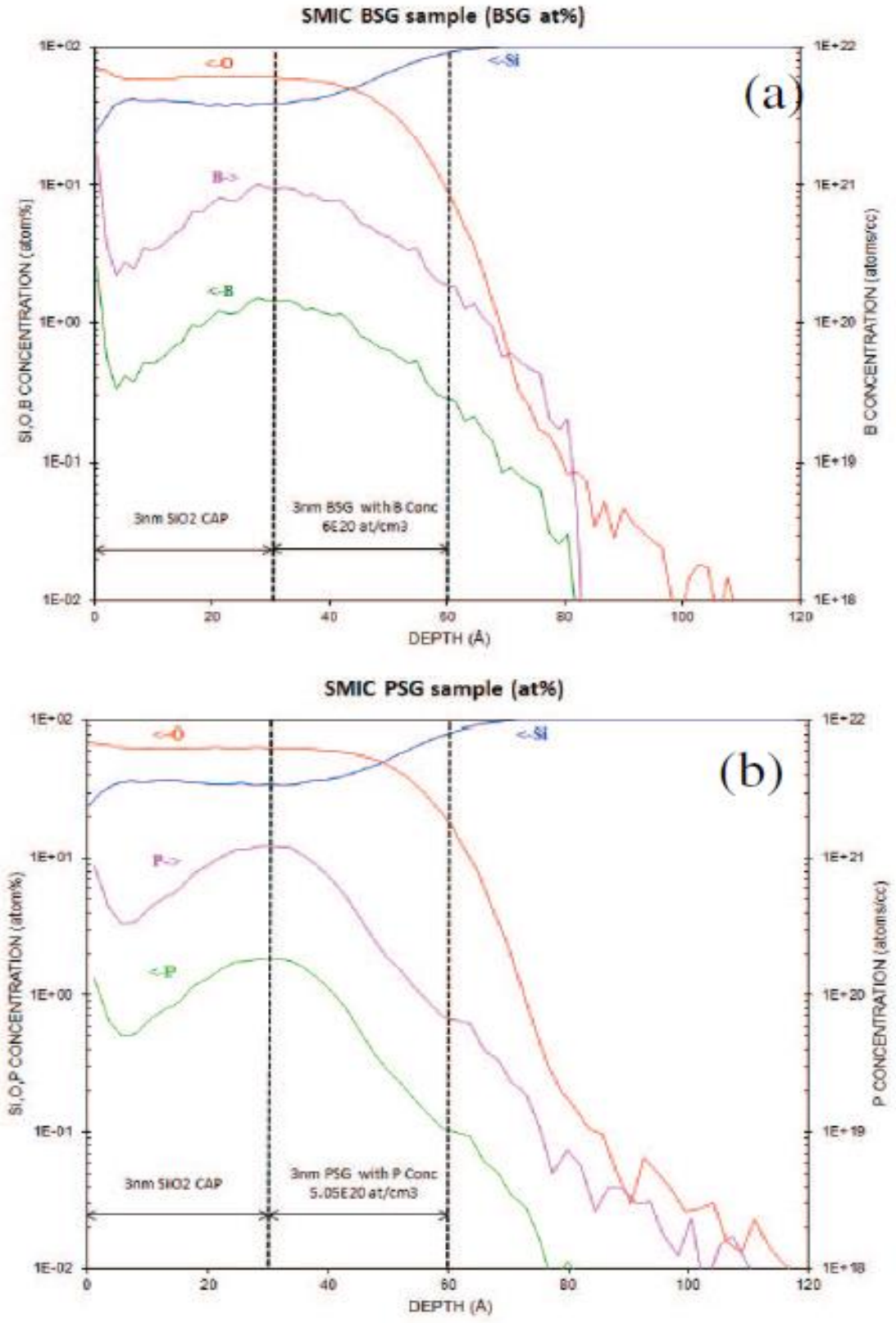

Fig. 3 Silicon dioxide boronsilicate glass Silicon substrate overlaying in (a) and Silicon dioxide phosphorous silicate glass Silicon substrate overlaying in (b) of SIMS profiles post-RTA

Figures 4(a) and (b) agree with earlier SIMS results obtained using B&P dispersion behaviour, displaying similar profiles but with a marginally lower concentration following the release of the boron silicate glass, and Boron

and phosphorus signal the phosphorous silicate glass. Films as a result of sputtering. A significant engineer repair work will be necessary to obtain the proper dopant concentration and device performance profile in the future, such as overhead and i-dopant. Torture, aneal state, and. The B / P distribution in the sub-fin may be as diverse as the Si wafers distribution.

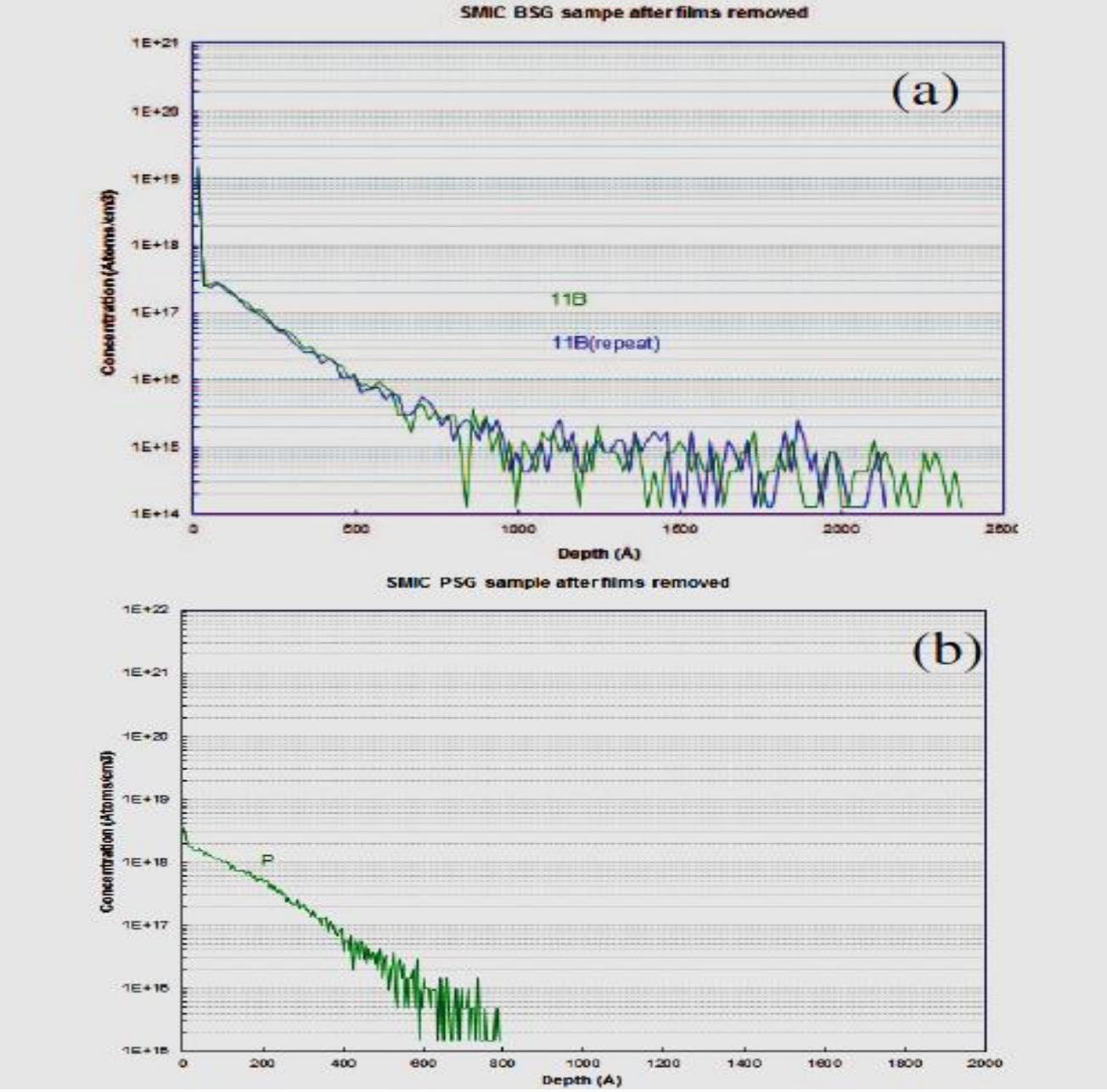

Fig. 4 After removing the Boron silicate glass(a) and Phosphorous silicate glass (b) layers and adding SiO2, SIMS profiles for Si substrates were developed

2.2. Flow-Control of Chemical vapour deposition

Conventional techniques significantly constrain the performance of filling the gap generation smaller than 14nm. It might be because, in this generation, the 'V' shape profile is difficult to perceive due to its particular integration flow. Their ongoing use in advanced technology nodes is additionally constrained by the specific criteria for Pre-Metal Dielectric, Sidewall angle, and STI channel profile from the HARP process. A re-entry gap is needed to close the gap in the planned trench's SiGe or SiC epi-layer that resulted from the PMD layer, as shown in Figure 5 below.

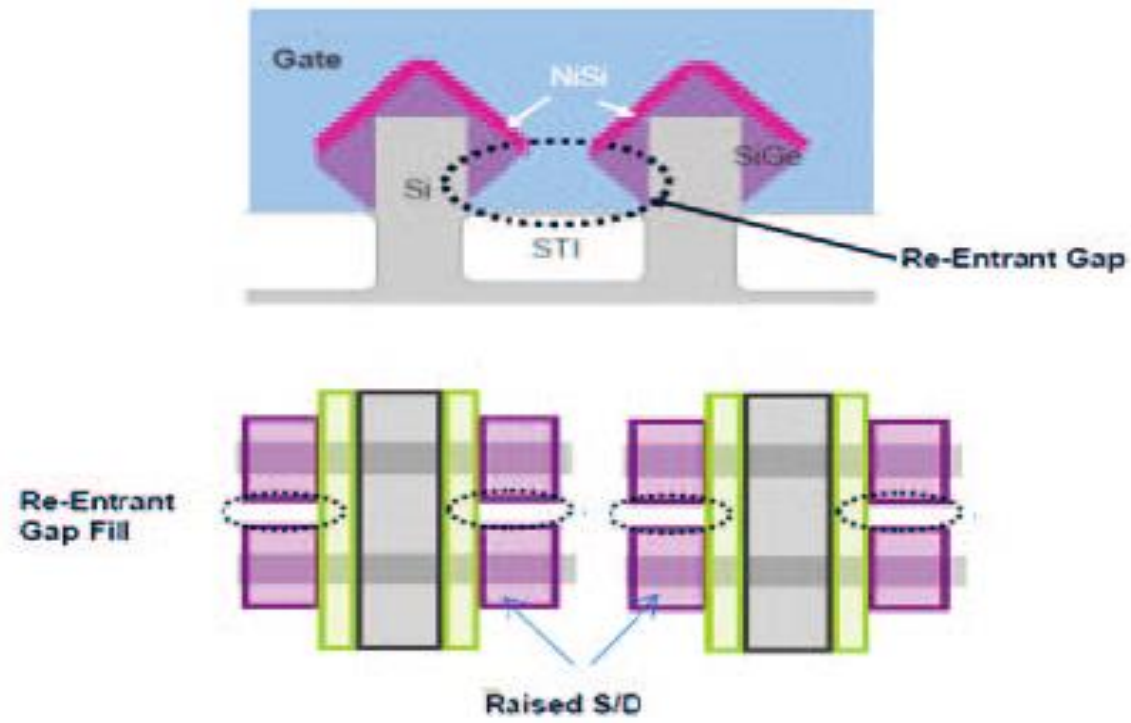

Fig. 5 Re-entrant gaps for PMD gap-filling

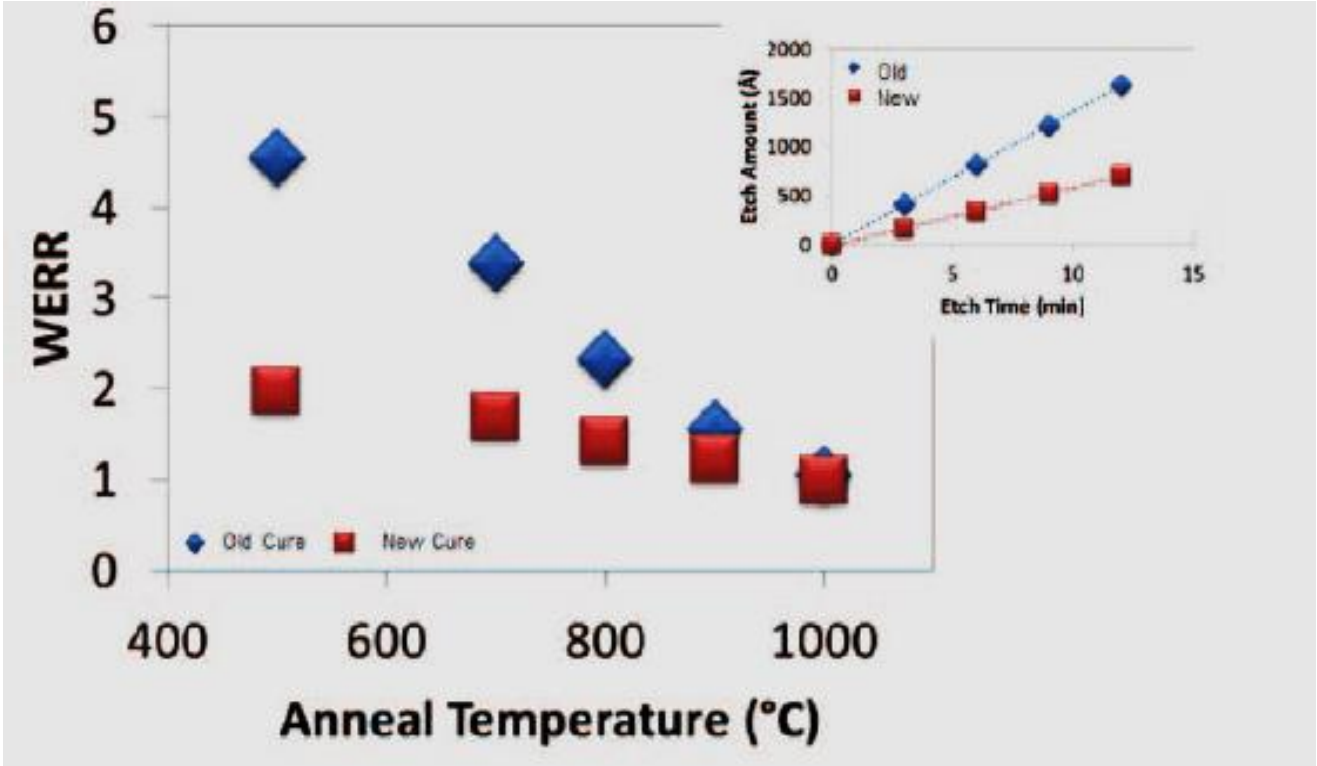

Fig. 6 Comparison of WERR samples on blanket wafers of flowable chemical vapour deposition silicon dioxide SiO2 that were annealed using various techniques.

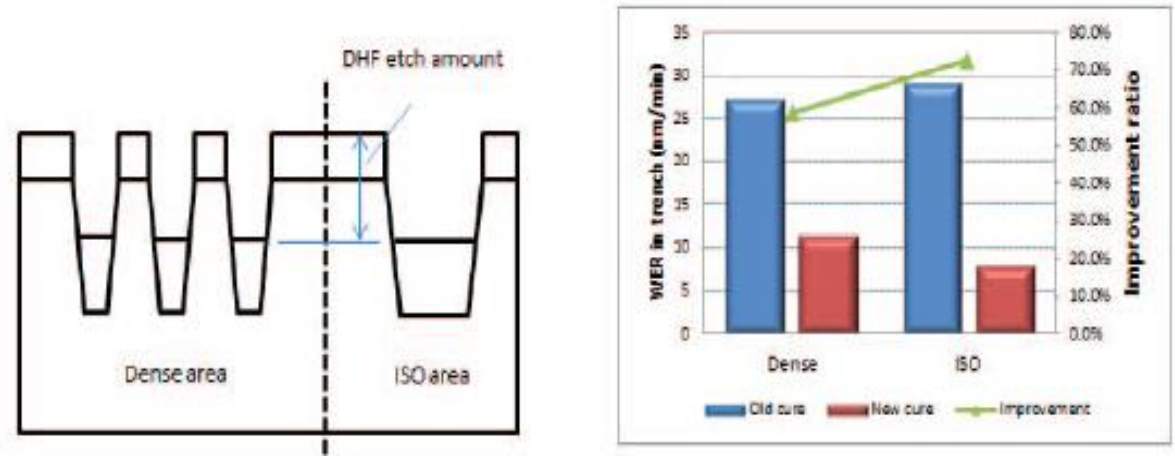

Fig. 7 WERR comparison for samples of SiO2 deposited by FCVD in trenches (both in populated and remote areas) and annealed using various techniques

The FCVD capacity-closing method has been enhanced in this regard, and gap-filling procedures have taken place for STI and ILD in dielectrics with sub-14 nm. Placement, treatment, and integration are the three primary phases of the conventional FCVD process. Deposition in the first stage refers to filling the space left by the precursor between the active radicals' NH * and flowing polymers. Maintaining the deposition reaction at a temperature that will boost the flow across the far-off plasma system is important. The second phase of the current normal oxide conversion process is carried out at a temperature between 100 and 200 °C, where solid SiO2 may be well generated.

After treatment, step-by-step heating moves up a level temperatures (ex:450-650 C) is required to reduce oxidation to comply with the internal layer structure of the channel (e.g., high altitude). The development of canal film material, CD loss, line bending, and other issues remain for the FCVD method despite its widespread adoption and high volume production of sub-14nm dielectrics.

The following generation of treatments has been created to deal with these issues. In essence, a new healing procedure combines Si-H with low temperature to create Si-Si for non-heat treatment. The new healing boosts Si and reduces FCVD as a film applied under low pressure compared to traditional therapeutic methods.

Film density and content before conversion/year. Wet Etch Rate Ratio, or WERR, is a measure of film density. The film is thick when the humidity is low, and vice versa. Figure 6 illustrates how samples subjected to a novel treatment at temperatures lower than 600 °C demonstrated a more than 50% reduction in WERR on clothing wafers compared to samples subjected to standard therapies, enabling the low-temperature budget.

A deep channel has helped the quality of the same movie improve, as seen in Fig. 7: The WERR is decreased from 25 nanometers per minute to 10 nanometers per minute for SiO2 objects placed in a dense region under the same adhesive circumstances and from 30 nanometers per minute to less than 10 nanometers per minute for SiO2 in one location. . Additionally, Si dislocation, which is frequently linked to a considerable slowdown in the normal process, has been significantly reduced as a result of the film thinned at a lower rate of stress.

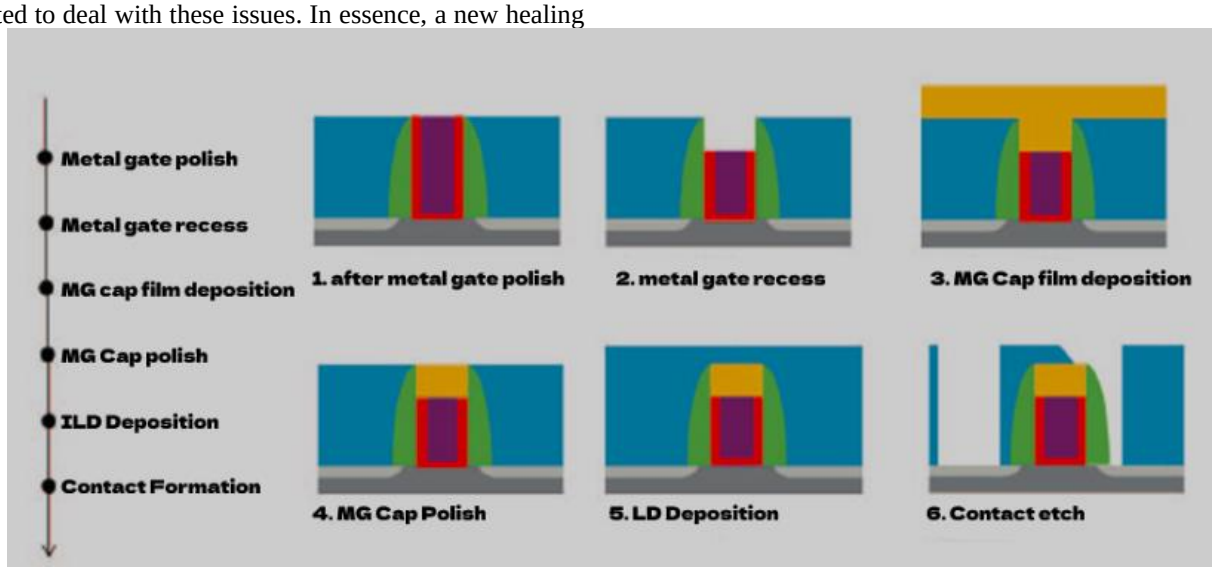

Fig. 8 Cartoon phase diagram for adopting a SAC

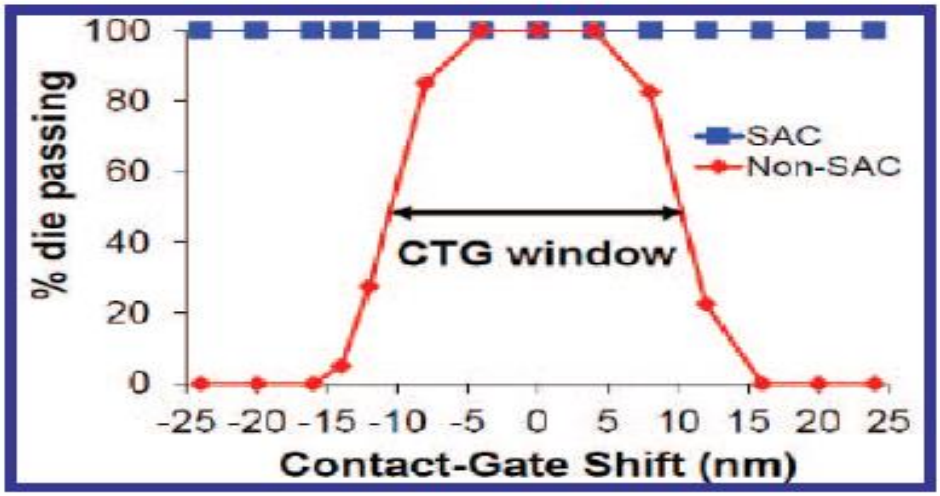

Fig. 9 Comparison of the Gate shift for SAC and Non-SAC from CT

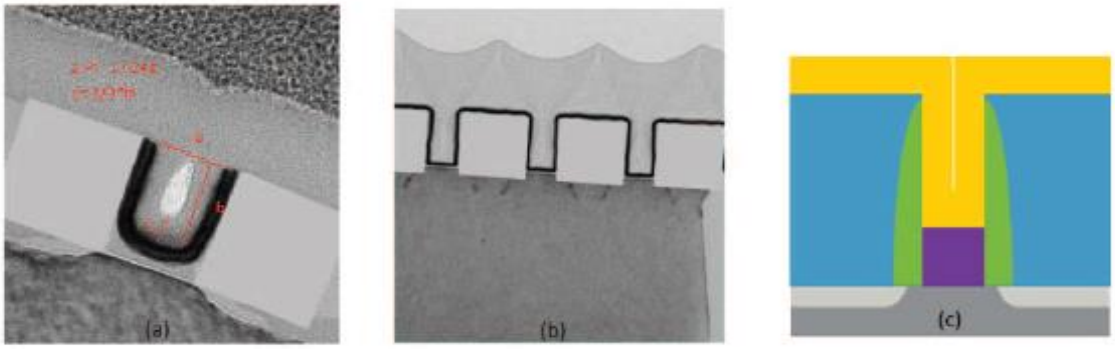

Fig. 10 shows a schematic of metal gate CAP, PECVD, HDP, and ALD nitride materials

2.3. The Use of Nitride for Self-Aligned Contact

To prevent potential crop losses caused by short gate contact, precise contact control (CT) to gate tightness is required as gate height is significantly reduced to 14 nm and below. Therefore, the overlay threshold between the gate network is intended to be developed through an alignment contract (SAC). Applying the SAC method requires additional procedures such as installing an after-gate adjustment, gate capping film, and polishing a metal gate broke (as shown in Fig. 8). The limit of CT overlay on the gate is very high, although the integration difficulty increases. According to the study,[8] the lithography process was most tolerated when the gate area changed from 20 to 10nm, as illustrated in Figure 9.

In this work, self-portrait films of nitride approach, for using the material for metal gate SI_3N_4 film is preferred because it is excellent for interlayer dielectric film and exceptional CMP compatibility. Installing SAC SiN can be done in many ways, including (HDP-SiN), (ALD-SiN), and (PE-SiN).

The PE-SiN film was initially employed in a typical wafer with a 22-aspect ratio to assess gap fill performance. The largest void issue is found in the region about 1/3 of the distance from the ditch's bottom to its top (as illustrated in Fig. 10(a)). To limit the negative impact in two different ways, a continuous setup of the process with crucial gas measurement parameters, pressure, and strength is necessary. One is to ensure that the void is buried in the canal's lowest level and that it does not reappear after CMP. Another option is to alter the top void to ensure that it will be completely eradicated during CMP.

The construction properties of HDP nitride are also being researched due to the space limitations of PE nitride. Even the additional challenge's aspect ratio in Fig. 10 might be used to fill a blank space in the building (b). However, plasma damage worries are raised during implementing good plasma to the metal gate. As a result, Another possible option for the SAC application is ALD nitride.

Emptiness can be reduced since ALD is a commitment to self-limitation. In terms of the plan, the seam is still present and cannot be avoided, which could be problematic. Table I below provides an overview of the benefits and drawbacks of those three procedures. The

integration scheme heavily influences the need to study the device wafer to choose the right processes thoroughly.

SiN Process comparison of various methods for self-alignment contract (**SAC) application**

1. Traditional mature process for PE-SiN

It has Low cost, good film quality, and limited capacity to patch gaps

2. Good gap fill capabilities for HDP-SiN,

1. Good picture quality, 2.- Damage from plasma,
3. Complex procedure

3. Seams persist despite conformal deposition used in ALD-SiN to minimise gap fill vacancies.

3. Conclusion

This paper explores that several innovative dielectric films are addressed; for example, Atomic Layer Deposition boron and phosphor silicate glass solid-state doping, flow able Chemical vapour deposition films, and nitride films for self-alignment contract application are being observed on textile waffles and 14nm FinFET technology. In a future lot of research ahead on carbon nanomaterials, graphite, etc

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