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Original Article

Three Phase Nine Level Modified NPC Grid Connected Inverter Topology with Proportional Resonant Based Control Strategy

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Abstract - *Existing literature predominantly focuses on operational analyses of single-phase modified five-level neutral-point-clamped (5L-NPC) inverter topologies in standalone configurations, with limited exploration of their closed-loop three-phase grid-connected (CL-3Ph-GC) counterparts. Critical gaps persist in addressing the interdisciplinary challenges of dynamic grid synchronization and harmonic interaction mechanisms inherent to three-phase architectures, necessitating holistic control frameworks that integrate advanced modulation strategies with grid compliance protocols to advance renewable energy integration. This paper proposes extending a three-phase, nine-level modified neutral point clamped grid-connected inverter (9L-MNPC-GCI) topology with a modified Proportional Resonant (PR) based control strategy. To generate nine levels in the pole voltage of 3-phase, a cascade connection of the modified 5L-NPC inverter topology with two cells has been considered, and it provides the greatest level of the line voltage. Prior to grid synchronization, the operational principles and implementation of the three-phase standalone system are analyzed, emphasizing the application of the Unipolar Phase Disposition Pulse Width Modulation (UPD-PWM) technique to achieve precise voltage regulation and harmonic suppression in islanded configurations. Compared with the normal Phase Disposition (PD) PWM technique, the implementation of the UPD-PWM technique is less. The same UPD-PWM technique has been incorporated at the end stage of a PR-based control strategy in 3Ph-GC. The entire PR-based control strategy is simpler than the conventional dq-frame control strategy. The study comprehensively examines the critical objectives of Active Power Control (APC), Reactive Power Control (RPC), and grid current harmonic mitigation within a CL-3Ph-GC. Utilizing the PLECS simulation platform, dynamic operational scenarios are employed to evaluate system performance under varying grid conditions.*

Keywords - *Modified neutral point clamped, Grid-connected inverter, Proportional resonant controller, Pulse width modulation, Active power and reactive power.*

1. Introduction

Rising global energy demand has increased fossil fuel use, worsening environmental damage from greenhouse gas emissions [1]. As a result, renewable energy resources are gaining attention for their efficient, low-pollution power generation [2]. The advancement of energy extraction efficiency in renewable systems has catalyzed the innovation of sophisticated control architectures and adaptive tracking algorithms designed to maximize power yield from inherently variable energy sources, as demonstrated in [3, 4]. Multilevel Inverters (MLIs) have emerged as a prioritized topology in power conversion research due to their inherent advantages, including high voltage handling capacity, enhanced efficiency through reduced switching losses, mitigated Electromagnetic Interference (EMI), and superior power quality enabled by their multi-level output topology, as evidenced in [5, 6]. MLI topologies serve as critical components in grid-integrated Renewable Energy Systems (RES) due to their scalability and compatibility with high-power applications [7]. Contemporary research prioritizes architectural simplification of MLIs, emphasizing the reduction of active switches and gate driver circuits to minimize system complexity, operational costs, and footprint while preserving performance in grid-tied configurations [8].MLIs are used in power systems for their high power quality, rating, low harmonic distortion, and EMI [9]. The most common industrial topologies are neutral Point Clamped (NPC), Flying Capacitor (FC), and cascaded H-

bridge (CHB) [10]. MLIs are increasingly favored in medium- and high-power energy conversion systems due to their inherent capability to synthesize high-fidelity output waveforms at reduced switching frequencies. This operational characteristic enables optimal harmonic performance while minimizing switching losses, making MLIs particularly advantageous for applications requiring stringent power quality and scalable deployment in grid-tied architectures, as highlighted in [11]. The conventional NPC inverter topology demonstrated superior performance in cascaded configurations, achieving minimized current Total Harmonic Distortion (THD) through its multi-level voltage synthesis. However, its commercial viability in grid-tied systems remains constrained by prohibitively high component counts, particularly switching devices and associated auxiliary circuitry, as noted in [12]. These limitations underscore ongoing research imperatives to refine modern MLI architectures, focusing on cost reduction, topological simplification, and enhanced grid compliance to mitigate inherent limitations in voltage balancing, fault tolerance, and dynamic response for renewable integration, as emphasized in [13].

MLIs have been comprehensively evaluated in contemporary literature through holistic assessments of their structural benefits, operational classifications, and inherent limitations, alongside their pivotal role in optimizing energy conversion efficiency within contemporary power infrastructures [14]. Emerging modified MLI configurations are gaining prominence in RES due to their synergistic advantages in cost-effectiveness, compact form factor, harmonic suppression, and enhanced conversion efficiency, positioning them as enabling technologies for sustainable grid integration [15]. Modulation techniques for MLIs can be categorized into different types of carrier-based PWM techniques [16]. The PD-PWM technique is more popular in obtaining better THD [17]. In [18], the single-phase cascaded NPC and CHB-based 7-level inverter topology is explained. In [19], a 3-phase 9-level inverter topology with PD-PWM technique is discussed. However, the PD-PWM technique needs more number of triangular carriers, and along with this, execution time also increases. Cascaded configurations of conventional NPC inverters enable 9-level voltage synthesis, albeit at the expense of elevated semiconductor device count and associated complexity in auxiliary circuitry [20]. Prior studies such as [21, 22] detail single-phase five-level MNPC inverter architectures, though their analyses remain confined to standalone operation, omitting critical evaluations of grid-tied functionality. Similarly, works in [23, 24] explore three-phase implementations of five-level topologies. Yet, their scope remains restricted to five-level output configurations without extension to higher voltage tiers or systematic integration with grid compliance protocols. These gaps highlight the need for advanced MLI designs for modern renewable energy systems to harmonize scalability, cost-effectiveness, and grid synchronization capabilities. Building upon the architectural framework established in [21], this paper presents a three-phase, nine-level inverter topology capable of seamless operation in both standalone and Grid Connected Modes (GCMs). Drawing on theoretical insights from [25, 26], an enhanced Proportional-Resonant (PR) control strategy synergistically integrated with UPD-PWM is developed to facilitate precise power regulation, harmonic suppression, and dynamic grid synchronization in nine-level grid-interfaced applications. This novel control architecture addresses the limitations of prior works by unifying advanced modulation techniques with adaptive feedback mechanisms, thereby optimizing harmonic performance, switching efficiency, and transient stability across dual operational paradigms. The paper's organisation in Section 2 gives the operation of the proposed 3-phase 9L-MNPC inverter topology. In Sections 3 and 4, both standalone and grid operations have been explained respectively. The comparative studies have been discussed in Section 5. Finally, conclusions are reported.

2. Description and Operation of Proposed 3-Phase 9L-MNPC-Inverter Topology

To generate 9 levels, the conventional single-phase cascade connection of NPC inverter topology needs a large number of semiconductor devices, as depicted in Figure 1. By considering [21], the extension of a 3-phase 9L-MNPC-GCI configuration has been proposed in this paper with a cascade connection of two 5L-MNPC inverter topologies. This topology consists of 12 discrete IGBTs with diodes, 2 bidirectional switches, 4 discrete diodes, and 4 equal DC sources per phase. At the end, the inductor filter (Lg) and grid are connected. The respective proposed 3-phase circuit diagram of a 9L-MNPC-GCI topology is depicted in Figure 2. The switching arrangement is represented in Table 1. From this, it is concluded that in every state, only six switches are conducted to produce 9L-pole voltage, and hence, this topology will be able to generate 17-level line voltage in the output. The enhanced voltage synthesis capability facilitates a reduction in passive filter requirements while inherently mitigating harmonic distortion in grid-injected currents.

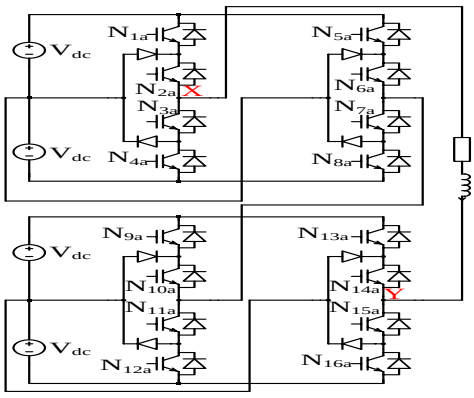

Fig. 1 Conventional 1-phase 9L-NPC inverter topology [20]

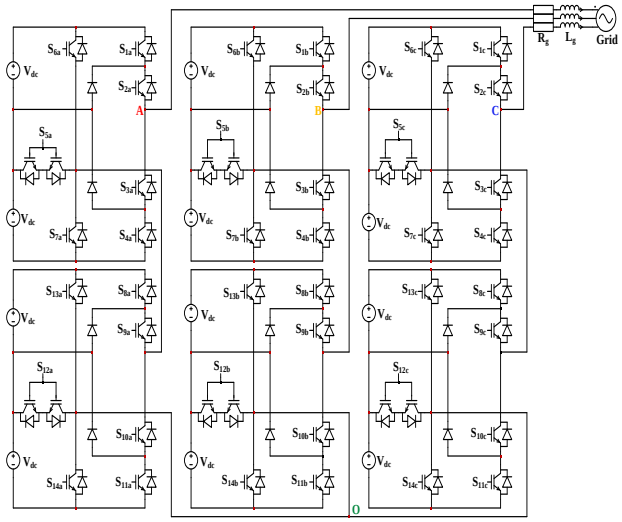

Fig. 2 Circuit diagram of 3-phase 9L-MNPC-GCI topology: proposed

Table 1. States of switches: 9-levels

S.No	Levels: V_{AO}	ON State Switches
1	0Vdc	S2,S3,S5,S9,S10,S12
2	+1Vdc	S2,S3,S5,S9,S10,S14
3	+2Vdc	S2,S3,S5,S8,S9,S14
4	+3Vdc	S2,S3,S7,S8,S9,S14
5	+4Vdc	S1,S2,S7,S8,S9,S14
6	-1Vdc	S2,S3,S5,S9,S10,S13
7	-2Vdc	S2,S3,S5,S10,S11,S13
8	-3Vdc	S2,S3,S6,S10,S11,S13
9	-4Vdc	S3,S4,S6,S10,S11,S13

This operational paradigm imposes asymmetric voltage stress distribution across semiconductor devices: selective switches (e.g., S6, S7, S13, and S14) endure elevated voltage stresses (2Vdc) during commutation while remaining switches operate under nominal stress (1Vdc) per phase. This asymmetric stress distribution necessitates optimized device selection to balance reliability and cost efficiency in the multilevel architecture.

3. Simulation Results: Standalone Operation with UPD-PWM Technique

The simulation parameters governing standalone operation are methodically outlined in Table 2. To synthesize a pole voltage waveform with a peak magnitude of ±400V, the DC link voltages are configured at 100V per source. Standalone operational validation is exclusively conducted under Resistive-Inductive (RL) load conditions to rigorously evaluate voltage regulation, harmonic performance, and transient stability in isolation from grid interdependencies. For any topology, the PWM technique is important in generating switching pulses. To generate 9 levels in the pole voltage, the conventional PD-PWM technique needs 8-triangular carriers; thereby, the implementation complexity also increases along with carriers.

Table 2. Simulation parameters

Standalone Mode: RL-Load	Grid Connected Mode (GCM)
Resistor(Load) =100Ω, Inductor(Load) =100mH, Switching Frequency =5kHz, and Vdc=100V.	Rg=0.01Ω, Lg=2.5mH, S=10kVA, Switching Frequency=10kHz, Vdc=100V, Vgrid=415V, and Grid Frequency=50Hz.

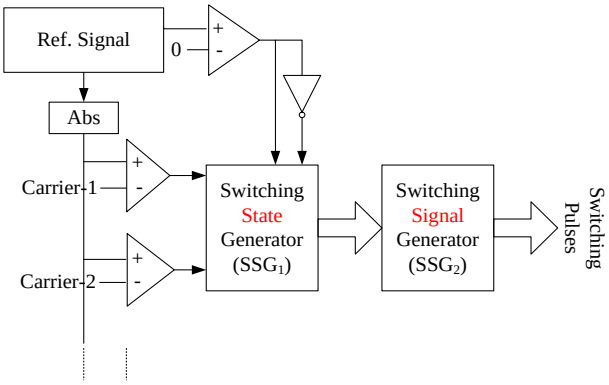

Fig. 3 Control diagram of UPD-PWM technique

To further reduce the complexity of the PWM stage, a UPD-PWM technique [11, 26] has been incorporated in this paper. In the UPD-PWM technique, the triangular carrier count can be reduced to half compared to the normal PD-PWM technique. This means that to generate 9 levels in the pole voltage, only 4 triangular carriers are needed, and thereby, the rest of the PWM implementation is also simple. This implementation leads to reduce the computational burden on the real-time processor units. The respective UPD-PWM technique is represented in Figure 3.

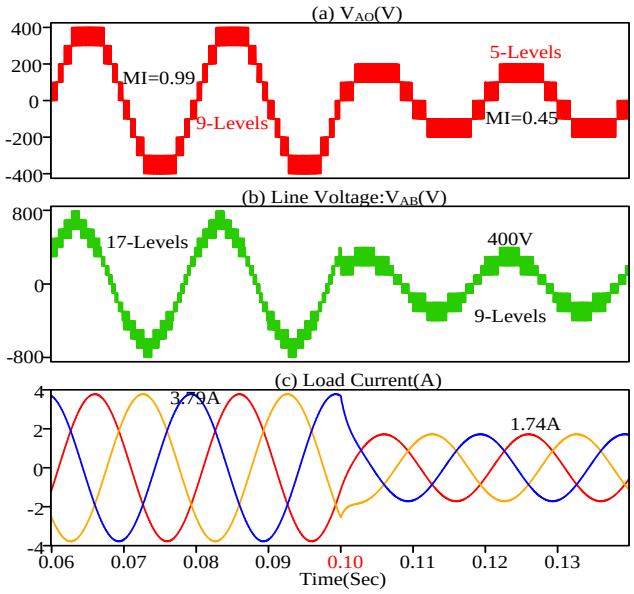

Fig. 4 Standalone results: MI=0.99 to 0.45 at t=0.1sec with RL-load

Following the implementation of the UPD-PWM technique on the three-phase 9L-MNPC inverter, a stepwise modulation index (MI) transition from 0.99 to 0.45 was introduced at t=0.1 S. The resultant dynamic response, as illustrated in Figure 4, captures the system's transient performance during abrupt MI variation, validating its closed-loop stability, voltage tracking accuracy, and harmonic attenuation capabilities under dynamic modulation conditions. In this, Figure 4 (a) represents the pole voltage (VAO) changes from 9 levels to 5 levels with peak values of ±400V and ±200V, respectively. Figure 4 (b) represents the line voltage changes from 17 to 9 levels with amplitudes of ±800V to ±400V. Figure 4 (c) shows the load current waveform with peak values of 3.79A to 1.74A. Finally, this UPD-PWM technique is effectively worked along with dynamics.

4. Simulation Results: Grid Connected Mode (GCM)-Modified PR-Based Control Strategy

The simulation parameters governing GCM are systematically detailed in Table 2. For 3Ph-GC systems, the minimum DC-link voltage constitutes a critical design parameter derived from the grid voltage amplitude to ensure uninterrupted power transfer and synchronization. Based on the empirical relationship Vdc, min=1.63×Vgrid, a minimum DC-link voltage of 676.45V is mandated to sustain stable operation under nominal grid voltage conditions. For safety reasons and other constraints, a reasonable DC-link voltage=700V/800V is required; hence, each DC source magnitude=100V is needed in this topology. Finally, with switching operation, the normal pole voltage gives ±400V, and the normal line-to-line voltage gives ±800V/±700V.

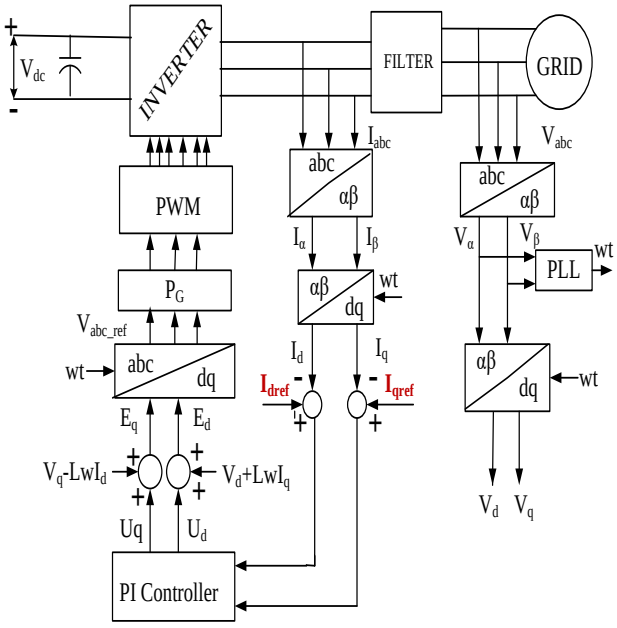

Fig. 5 Conventional dq-frame control strategy: 3- Ph GC [3, 10]

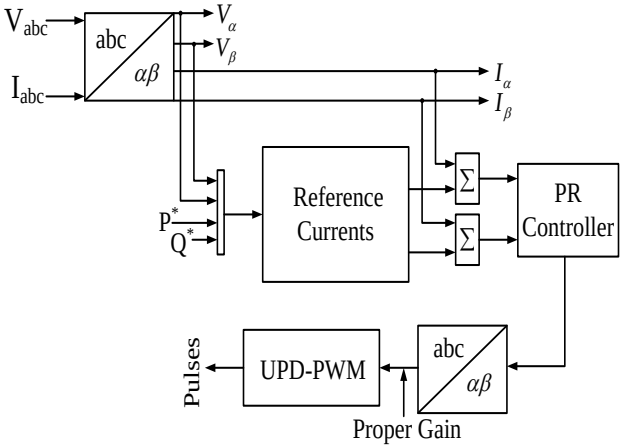

Fig. 6 Modified PR-based control strategy with UPD-PWM technique: proposed

For any 3Ph-GC, the closed-loop control strategy is important to achieve all grid objectives. The conventional dq-frame control strategy is depicted in Figure 5, which gives an effective solution for all 3-phase GCI topologies. However, its implementation needs more transformations, Phase Locked Loop (PLL) requirements, and more number of Proportional Integral (PI) controllers. To reduce the control complexity, a PR-based control strategy with the UPD-PWM technique has been proposed in this paper, and it is represented in Figure 6. The basic input points for implementing the PR-control strategy are taken from [25]. In the PR control strategy, first sense the both grid voltage and grid current of all phases. By using abc to alpha-beta transformation, convert abc quantities into alpha-beta quantities of both grid voltage and grid current.

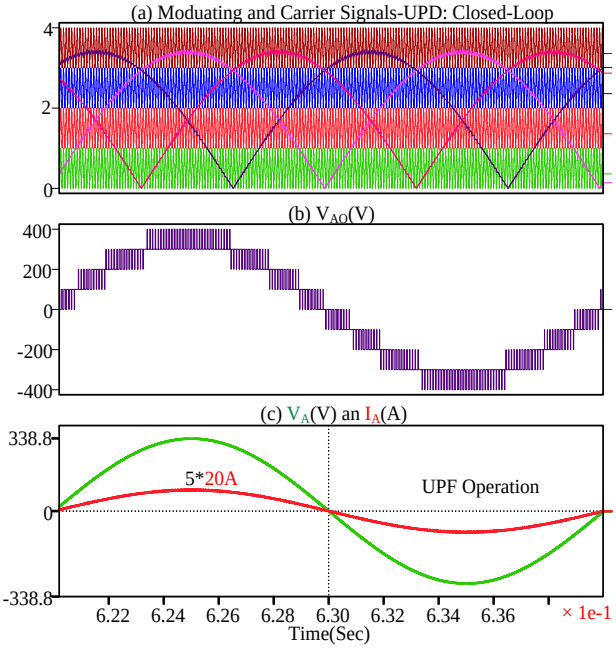

Fig. 7 GCM results: zoomed view-UPF of grid

By taking the inputs of Vα, Vβ, P*, and Q*, the reference currents are generated [25]. These reference currents are compared with Iα and Iβ. The obtained output signals are fed with the PR controller, and inherently, it almost provides zero steady-state error. After the PR-controller, the obtained alpha-beta quantities are converted into an abc frame. Next, to obtain the desired modulating signals, a proper gain (normalization) should be provided before the UPD-PWM technique. In this implementation, no PLL is required. This entire implementation is simple compared with the conventional dq-frame control strategy, and it is a more effective control solution for all 3-Ph GCI topologies. After applying the PR-based control strategy, the following simulation results are obtained. Figure 7 represents a zoomed view of the unity power factor (UPF) of the grid with P*=10kW and Q*=0VARs.

Figure 7 (a) represents unipolar modulating and triangular carrier signals in a closed loop. Figure 7 (b) represents a 9-level pole voltage with peak values of ±400V. Figure 7 (c) shows the UPF operation of the grid with a peak value of injected grid current of approximately 20A. In this, the scaling factor=5 represents the visibility of the grid current properly, and a gain is provided at the scope. Figure 8 represents the UPF of the grid with step change of P*=10kW to 5kW and Q*=0VARs at t=1sec. Figure 8 (a) represents 3-phase grid voltages with peak values of ±338.8V. Figure 8 (b) represents injected 3-phase grid currents with peak values of ±20A and ±10A. Figure 8 (c) represents the UPF operation of the grid. Figure 8 (d) represents the 9-level pole voltage with peak values of ±400V.

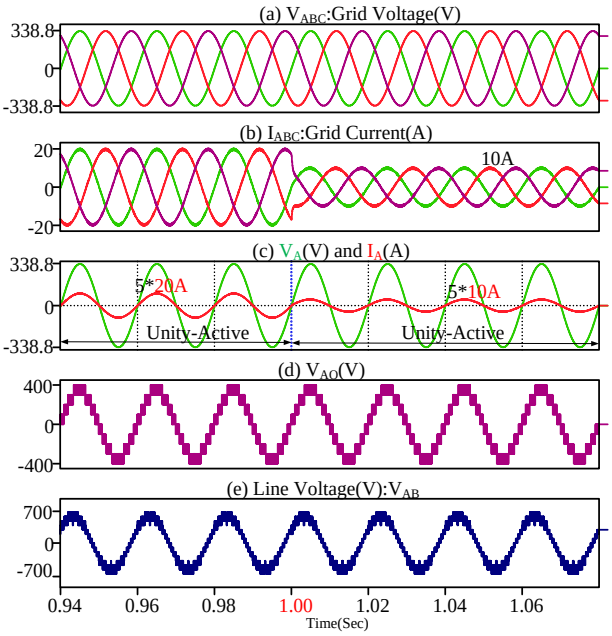

Fig. 8 GCM results: step change of P*=10kW to 5kW and Q*=0VARs-UPF operation

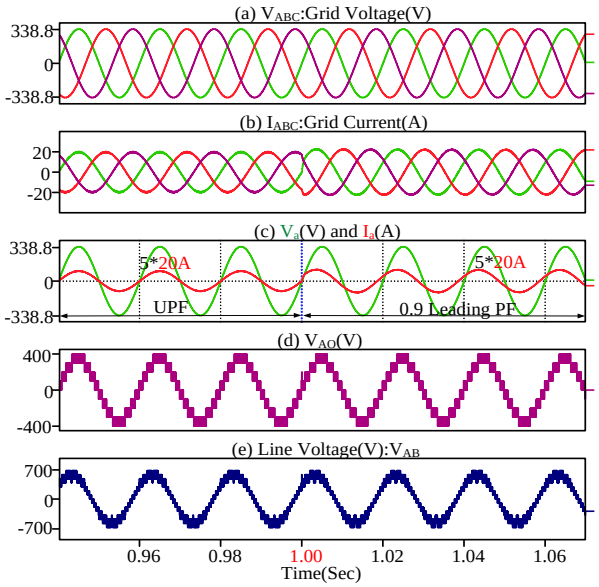

Fig. 9 GCM results: step change of PF=one to 0.9 leading

Figure 8 (e) represents the line voltage of the 15 levels with peak values of ±700V. The number of voltage levels depends on the injected grid current waveform w.r.to grid voltage. Figure 9 represents the step change of PF=1 to 0.9 leading. In this, P*=10kW (t=0 to 2sec) and Q*= 0VARs & -4843.22VARs (before t=1sec and after t=1sec) are considered to obtain unity and 0.9 leading PF. Figure 10 represents the step change of PF=1 to 0.9 lagging. In this, P*=10kW (t=0 to 2sec) and Q*= 0VARs and +4843.22VARs (before t=1sec and after t=1sec) are considered to obtain unity and 0.9 lagging PF.

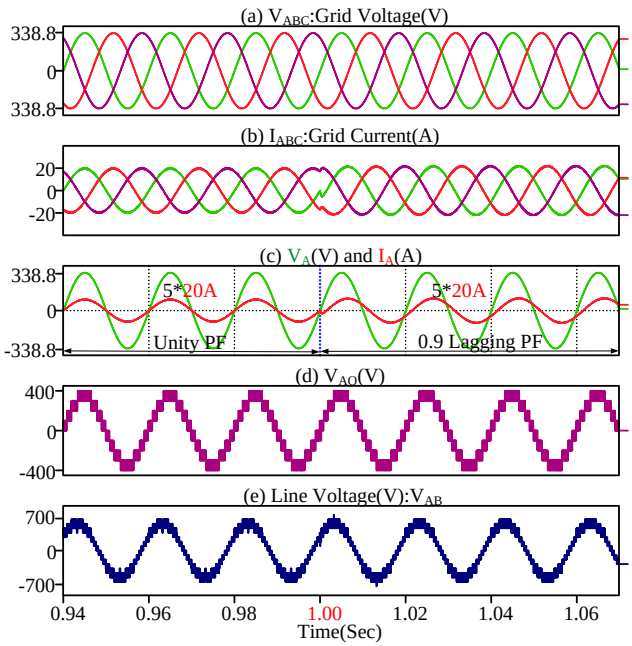

Fig. 10 GCM results: step change of PF=one to 0.9 lagging

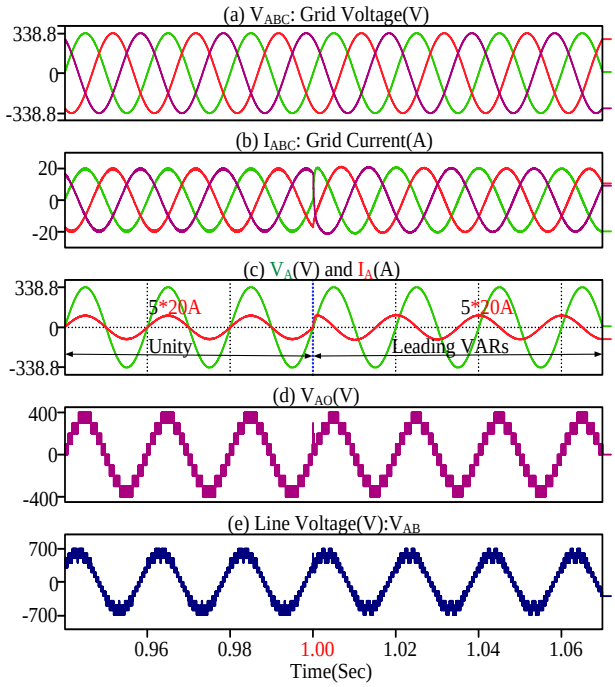

Fig. 11 GCM results: step change of UPF (active power) to leading VARs

Figure 11 represents the step change of UPF to leading VARs. In this, P*=10kW & 0kW (before t=1sec and after t=1sec) and Q*= 0VARs & -10kVARs (before t=1sec and after t=1sec) are considered.

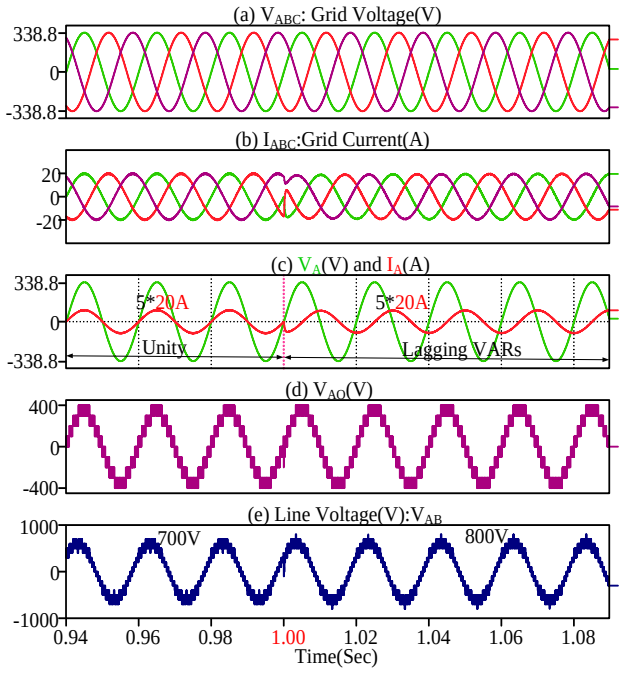

Fig. 12 GCM results: step change of UPF (active power) to lagging VARs

Figure 12 represents the step change of UPF to lagging VARs. In this, P*=10kW & 0kW (before t=1sec and after t=1sec) and Q*= 0VARs & +10kVARs (before t=1sec and after t=1sec) are considered. In this case, after t=1sec, the line voltage has 17 levels with peak values of ±800V. From all these dynamic case studies of GCI results, it is concluded that both APC and RPC have been achieved effectively with the proposed PR-based control strategy. Figure 13 represents the harmonic spectrum (HS) of pole voltage, which gives total harmonic distortion (THD) of 17.19% with peak value=400V.

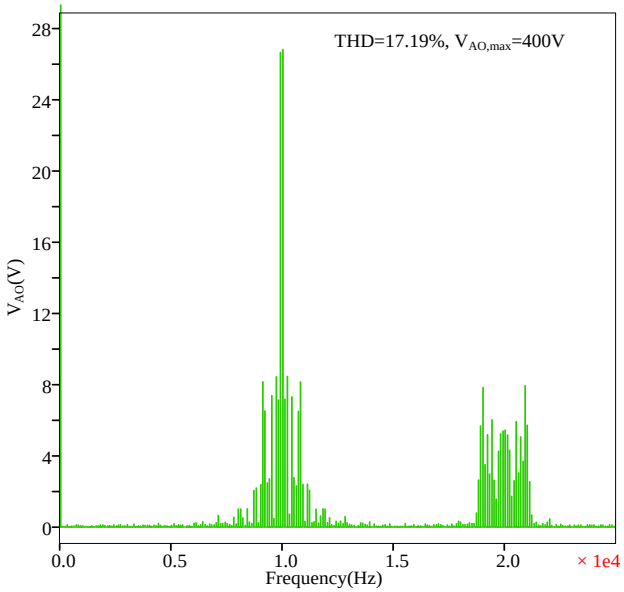

Fig. 13 HS of VAO under UPF operation (9-levels): GCM

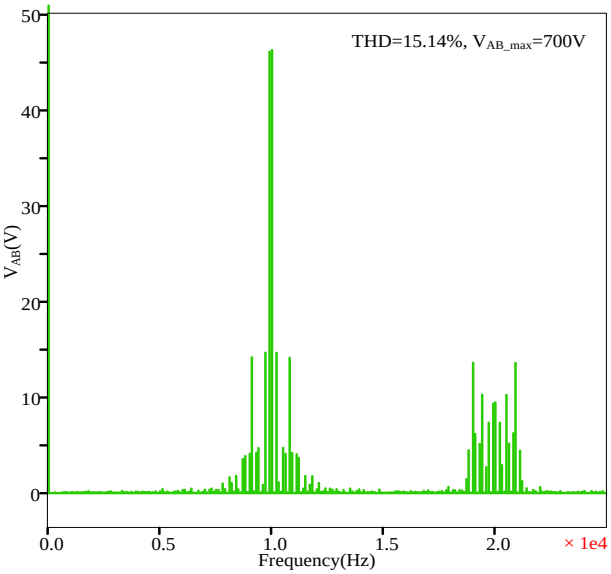

Fig. 14 HS of VAB under UPF operation (15- levels): GCM

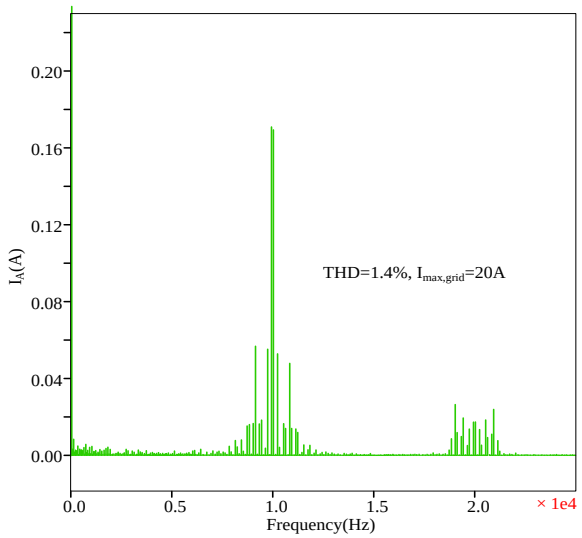

Fig. 15 HS of injected IA(A) under UPF operation: GCM

Figure 14 represents the HS of line voltage, which gives THD of 15.14% with peak value=700V. Figure 15 represents the HS of injected grid current, which gives THD of 1.4% with peak value=20A. From this result, the injected grid current has less harmonic distortion and effectively follows IEEE-1547 standards. Finally, all three-phase grid-connected objectives have been achieved through the proposed PR-based control strategy.

5. Comparative Study

Table 3 compares the conventional 9L-NPC topology and proposes a modified 9L-NPC topology w.r. to the semiconductor and DC sources count. From this, the proposed 9L-MNPC topology has a smaller number of semiconductor devices; hence, the cost will decrease. Table 4 presents a comparative analysis of conventional dq-reference frame control strategies and the proposed PR-based control architecture.

The results demonstrate that the modified PR-based strategy, synergized with the UPD-PWM technique, exhibits a streamlined implementation framework with reduced computational overhead, significantly alleviating the processing demands on real-time Digital Signal Processors (DSPs). This efficiency stems from eliminating complex coordinate transformations and adaptive frequency tracking inherent to dq-axis methods while retaining precision in harmonic suppression and dynamic grid synchronization.

Table 3. Comparative study-1 (topologies: per phase)

S. No	Description	Conventional 9L-NPC [20]	Proposed 9L-MNPC
1.	Number of IGBTs	16	12
2.	No. of Bidirectional Switches	00	02
3.	No. of Discrete Diodes	08	04
4.	No. of DC Sources	04	04

Table 4. comparative study-2 (control strategies)

S. No	Description	Conventional dq-Frame Control [3, 10]	Proposed PR-Control with UPD-PWM Technique
1	Vector Control	Synchronous Reference	Stationary Reference
2	Transformation Blocks	More	Less
3	No. of PI Controllers	Three	Zero
4	PWM	PD-PWM	UPD-PWM
5	Number of Carriers	Level-1	(Level-1)/2
6	PLL	Required	Not Required
7	Control Complexity	High	Low
8	Total Execution Time	More	Less

6. Conclusion

In this paper, a three-phase 9L-MNPC-GCI topology with a closed-loop PR-based control strategy has been explained. Before going to the grid connection, the standalone operation is also described, considering the UPD-PWM technique. This topology provides a line voltage of 17 levels with a peak value of 8Vdc; thereby, the grid filter size is also smaller. The proposed 9L-MNPC topology has a smaller component count than the conventional 9L-NPC topology, and the proposed PR-control strategy complexity is also less than that of the conventional dq-frame control strategy. The main objectives of APC, RPC, and less harmonic grid current distortion have been effectively achieved with different case studies using a modified PR-based control strategy. In the future, the three-phase topology work will be updated for STATCOM, AFER, etc., for different kinds of applications with different types of control strategies.

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