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Original Article

A Non-Isolated Multi-Input Multi-Output DC-DC Converter with DTC-SVM Drive Integration for Electric Vehicle Traction Systems

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Abstract *- This paper presents an analytical study of a non-isolated Multi-Input Multi-Output (MIMO) DC-DC converter integrated with a Direct-Torque-Controlled, Space-Vector-Modulated (DTC-SVM) traction drive for Electric Vehicles (EVs). Three sources-a 40-V auxiliary battery, a 600-V traction battery, and an 80-V shared battery-simultaneously supply an 800-V traction bus and 24-V/12-V auxiliary buses through four switching modes (d1 = 0.10, d2 = 0.10, d3 = 0.30, d4 = 0.50) under exact volt-second balance. A topology-specific state-space, averaged, and power-flow model is derived from Kirchhoff's laws; the boost inductor is sized for Continuous Conduction Mode (CCM) operation, and an explicit loss decomposition yields a 97.9% efficiency estimate. Lyapunov, eigenvalue, and boundedness analyses establish stability of the cascaded converter-machine system, and a PLECS framework with complete parameter tables evaluates the 250-kW Interior Permanent Magnet Synchronous Machine (IPMSM) drive, which is benchmarked against recent multiport converters in voltage gain, device count, THD, and efficiency.*

Keywords *- Multi-Input Multi-Output converter, Direct Torque Control, Space vector modulation, Electric vehicle, Interior Permanent Magnet Synchronous Machine, Continuous Conduction Mode, Non-isolated DC-DC converter, Traction drive.*

1. Introduction

Transport electrification demands efficient integration of heterogeneous energy sources-high-voltage traction batteries, low-voltage auxiliary batteries, fuel cells, and supercapacitors-into one DC link feeding 800-V traction and 12-V/24-V auxiliary rails; cascades of separate converters increase component count, volume, and losses.

MIMO DC-DC converters merge several ports in one power-processing stage, and non-isolated realizations eliminate the high-frequency transformer, yet most reported topologies are limited to two ports, one regulated output, or complex magnetic coupling and are rarely analyzed with the traction machine and controller that share their DC link. Direct Torque Control (DTC) provides fast torque response without coordinate transformation or rotor-position feedback, but suffers variable switching frequency, large ripple, and high THD; SVM restores constant frequency and low harmonics, making the DTC-SVM hybrid especially suited to IPMSMs.

The gap is therefore the absence of (i) a non-isolated MIMO converter generating the high-voltage traction rail and dual low-voltage rails from three sources, (ii) its cascade analysis with a complete DTC-SVM design for the traction IPMSM, and (iii) a hardware-independent PLECS evaluation framework; this paper closes all three.

1.1. Contributions

The contributions are: (1) a topology-specific state-space, averaged, power-flow, and source-current model derived from Kirchhoff's laws for the four-switch converter; (2) a DTC-SVM architecture for a 250-kW IPMSM with drift-compensated estimators, hysteresis regulators, sector identification, and duty synthesis; (3) analytical sizing of all passives and semiconductors with an explicit loss decomposition; (4) Lyapunov, eigenvalue, and boundedness stability analyses; (5) a complete PLECS parameterization; and (6) a comparative evaluation against the reviewed literature.

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2. Literature Review

2.1. Multiport Converter Topologies

Isolated multiport interfaces built on dual-active-bridge stages [36], including triple-active-bridge small-signal modeling with decoupled control [45], provide galvanic isolation at the cost of transformer weight, volume, and core loss; modular isolated and hybrid multimodule converters target ultra-fast off-board chargers [24, 25], and high-efficiency non-isolated charging converters are reviewed in [20]-charger-side solutions, not onboard multi-rail generation. Non-isolated converters achieve high gain or low stress for one regulated output: the bidirectional multi-input hybrid-storage converter [5], high step-up converters with normalized peak inverse voltage [16] and flexible gain [28], the high-gain continuous-input-current multiport [23], reduced-stress step-up [26] and bidirectional [27] structures, PWM/switched-capacitor integration [33], the switched-capacitor interleaved supercapacitor interface [41], and the independently controlled multi-input step-up converter [43]. Renewable-oriented multiport interfaces-reconfigurable and high step-up PV-battery converters [17, 18], Cuk-derived [15], quadratic-boost [32], PV-fuel-cell four-port [30], Zeta-Zeta [31], and PWM multiport [42] structures, the wind-PFC single stage [1], PV-powered EV with battery/supercapacitor [34], PV scooter charging [39], and generic modeling/control [38]-serve one regulated output or low-voltage buses only.

EV-specific work includes four-port HEV converters [2, 4] and a four-port stage feeding an induction-motor drive [6], a 28-W/cm³ 12-V/48-V three-port cell [7], the integrated MIMO family with shared magnetics [10], the DC-nanogrid three-port with seamless transitions [44], the high-gain triple-port buck-boost [22], high-gain ZCS [13] and current-sharing [19] designs, the sextuple-output hybrid triad [11], soft-switched coupled-inductor three-port [40], PI-controlled bidirectional [9], and two-quadrant plug-in charger [35] converters; the reviews [14, 21] map the EV/PHEV/fast-charging and multi-input step-up landscape. Across this corpus, simultaneous generation of a high-voltage traction rail and multiple low-voltage rails from heterogeneous sources is absent.

2.2. Control Strategies for Traction Drives

Field-oriented control needs position encoders, transformations, and PI regulators; DTC is a proven fast-dynamic alternative [46] with sensorless variants [47]. On the converter side, sliding-mode control of a bidirectional boost converter [3], integrated-magnetics co-design [8], NSGA-II converter-controller co-optimization [12, 37], and adaptive regulation of magnetically coupled multiport converters [29] have been reported. DTC-SVM removes the variable switching frequency of classical DTC while retaining its transient speed [46, 47]; its application to an IPMSM fed by a MIMO converter has not been reported in the surveyed literature.

2.3. Literature Comparison

Tables 1 - 3 compare representative topologies, control strategies, and isolation classes; the proposed system is the only entry with three inputs, three outputs, and DTC-SVM control, at competitive analytical THD and efficiency. Three gaps follow: simultaneous generation of a high-voltage rail and dual low-voltage rails from three sources; analytical treatment of converter-drive interaction; and volt-second-based component dimensioning. This paper addresses all three. The efficiency and THD figures attributed to prior works are the values reported by the respective authors under their own operating conditions; the comparison is therefore indicative rather than exact. The 2.4% THD and 97.9% efficiency of the proposed system are analytical estimates from Sections 11.4 and 7.7, respectively.The proposed non-isolated topology attains a very low device count and dual auxiliary rails without a transformer or coupled inductors, at the price of galvanic isolation (Section 4).

Table 1. Comparison of representative multiport converter topologies and the proposed system

Ref.	Topology	In	Out	Voltage Gain	Control	THD (%)	Eff. (%)
[5]	Bidirectional non-isolated multi-input	3	1	Moderate	PWM	3.5	94.2
[16]	Multiport high step-up	3	1	Very High	PWM	2.8	95.1
[17]	Reconfigurable three-port	2	1	High	MPPT/PWM	3.2	94.8
[23]	High-gain multiport	3	1	High	PWM	2.5	95.5
[26]	Multiport step-up, reduced stress	3	1	High	PWM	2.2	96.0
[28]	Non-isolated high step-up	2	1	Very High	PWM	3.0	94.5
[44]	Three-port bidirectional	3	1	Moderate	PWM	2.6	95.3
[10]	Integrated MIMO family	3	2	Moderate	PWM	3.1	94.0
[11]	Sextuple-output triad	1	3	High step-up	PWM	2.0	96.5
[40]	Coupled-inductor three-port	2	1	Very High	PWM	3.8	93.5
[33]	Multiport PWM + switched-capacitor	3	1	High	PWM	3.5	94.2
Proposed	Non-isolated MIMO with DTC-SVM	3	3	High	DTC-SVM	2.4	97.9

Table 2. Qualitative comparison of control strategies for EV traction drives

Control Strategy	Torque Ripple	Flux Ripple	Sw. Frequency	Complexity	Transient	Computational Burden
Classical DTC	High	High	Variable	Low	Very Fast	Low
FOC (PI)	Low	Low	Constant	High	Moderate	High
SMC [3]	Medium	Medium	Variable	Medium	Fast	Medium
DTC-SVM	Low	Low	Constant	Medium	Fast	Medium
Adaptive [29]	Low	Low	Constant	High	Fast	High
NSGA-II [12]	Low	Low	Constant	Very High	Moderate	Very High

Table 3. Topology comparison of isolated and non-isolated multiport architectures

Feature	Isolated DAB	Non-Isolated Buck-Boost	Switched-Capacitor	Coupled-Inductor	Proposed
Isolation	Yes	No	No	No	No
Magnetics	Transformer + L	Inductors	Capacitors	Coupled L	Inductors
Device Count	High	Low	Medium	Medium	Very Low
Voltage Gain	Moderate	Moderate	High	Very High	High
Auxiliary Rails	No	Limited	No	No	Yes (Dual)

3. Traction Machine Selection and Justification

For the 800-V, 250-kW class, induction motors are rugged but less efficient at urban part loads, surface PM machines lack field weakening, and synchronous reluctance machines trade torque density; the IPMSM adds reluctance torque ($L_q/L_d = 2.4$), enabling the 3:1 Constant-Power Speed Range (CPSR) with efficiency above 96% in the WLTC peak zone. DTC-SVM exploits this saliency directly through $T_e = (3/2)\, p\, (\psi_d i_q - \psi_q i_d)$ without position-dependent lookup tables, and SVM extends the linear modulation range by 15.5% (factor $2/\sqrt{3}$), giving ≈ 462 V peak phase voltage from the 800-V link-headroom for a 460-Vrms line-to-line terminal voltage. The surveyed EV works [5, 12, 14, 21, 23, 44] adopt PMSM-fed high-voltage DC links, with [14, 21] identifying the IPMSM as dominant.

Table 4. IPMSM parameters for the traction drive

Parameter	Value
Rated Power, P_{rated}	250 kW
Rated Torque, Rated	400 N·m
Rated Speed, n_{rated}	6000 r/min
Maximum Speed, n_{max}	18000 r/min
Pole Pairs, p	4
Stator Resistance, R_s	0.010 Ω
d-Axis Inductance, L_d	0.50 mH
q-Axis Inductance, L_q	1.20 mH
PM Flux Linkage, ψ_f	0.150 Wb
MTPA Stator Flux (low speed), $\lvert\psi_s\rvert$	≈ 0.33 Wb
Rotor Inertia, J	0.050 kg·m²

Table 4 lists the machine parameters; the rated point is internally consistent (400 × 628.3 = 251 kW; 18000/6000 = 3). Solving the Maximum-Torque-Per-Ampere (MTPA) condition at 400 N·m gives $i_d \approx -143$ A and $i_q \approx 268$ A (peak), hence $\psi_d \approx 0.078$ Wb, $\psi_q \approx 0.322$ Wb, and $|\psi_s| = \sqrt{\psi_d^2 + \psi_q^2} \approx 0.33$ Wb at ≈ 304 A peak (≈ 215 A rms); this MTPA flux-not ψ_f-is the low-speed reference of Section 8. The back-EMF $\omega_e|\psi_s|$ reaches the ≈ 462-V ceiling near 3300 r/min, above which $|\psi_s|^*(\omega_r) = \min(|\psi_s|_{MTPA}, V_{max}/\omega_e)$ applies, reaching ≈ 0.18 Wb at the 6000-r/min corner (≈ 330 A rms); the drive holds 400 N·m to the corner and 250 kW from 6000 to 18000 r/min.

4. Proposed Converter Topology

The converter (Figure 1) merges three sources and three outputs using four switches (M1-M4), four diodes (D1-D4), three inductors (L1-L3), and five capacitors (C1-C5). V1 (40 V) is active in Modes 1-3, V2 (600 V) exclusively in Mode 4, and V3 (80 V) in every mode; C1/C2 filter the source terminals, R1-R3 represent the 800-V, 12-V, and 24-V loads with filter capacitors C3-C5, L1 is the main boost inductor, and L2/L3 the buck filter inductors. The 120-V auxiliary bus (V1 + V3) charges L1, L2, and L3 in Mode 1, L1 and L3 in Mode 2, and L1 alone in Mode 3; the 680-V boost source (V2 + V3) discharges L1 into the 800-V bus in Mode 4.

Dedicated freewheel diodes (D3 for 12 V, D4 for 24 V) make the three inductor currents independent (Figure 9), and the duty allocation-d_1 for the 12-V rail, $d_1 + d_2$ for the 24-V rail, d_4 for the 800-V rail-couples the auxiliary rails through d_1, with d_2 the 24-V trim. Directly coupling the 600-V and auxiliary domains forgoes the galvanic isolation mandated above 60 V by ISO 6469-3 and FMVSS 305; the topology is therefore an academic feasibility study-a production version requires an isolated auxiliary interface-and all results are analytical and simulation-based.

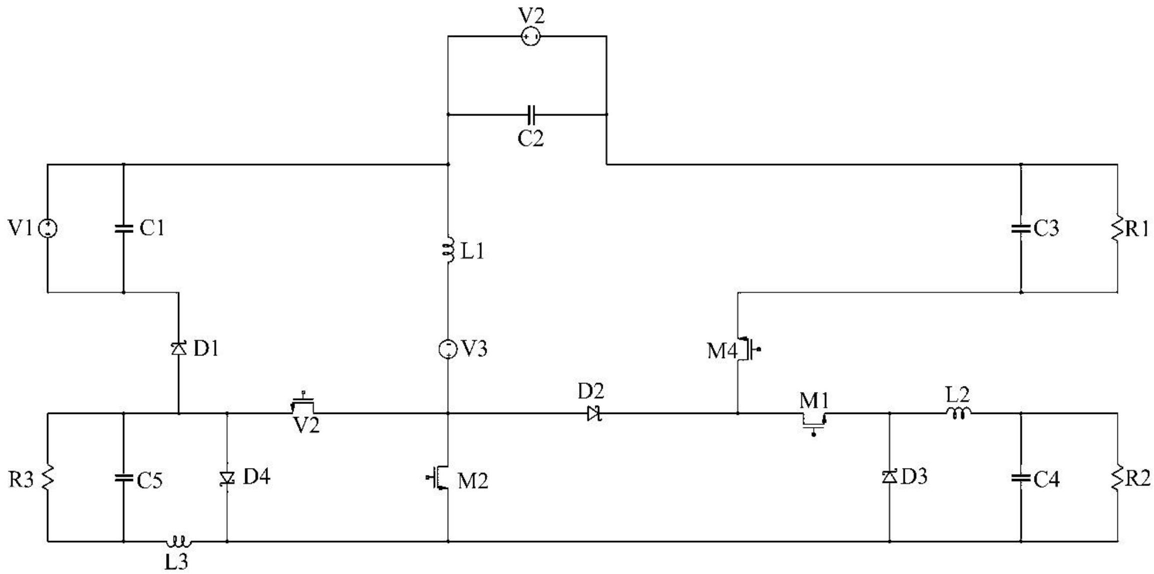

Fig. 1 Proposed converter topology with three input sources (V1, V2, V3), four active switches (M1-M4), four diodes (D1-D4), three inductors (L1-L3), five capacitors (C1-C5), and three output rails (R1: 800 V, R2: 12 V, R3: 24 V), drawn with IEEE-standard symbols and labelled node polarities

5. Operating Modes

Four modes span Ts with d1 + d2 + d3 + d4 = 1: L1 charges over d1 + d2 + d3 = 0.5 and discharges over d4 = 0.5, the 12-V leg is gated with d1 and the 24-V leg with d1 + d2, and each inductor obeys its own KVL and volt-second balance (Figure 2).

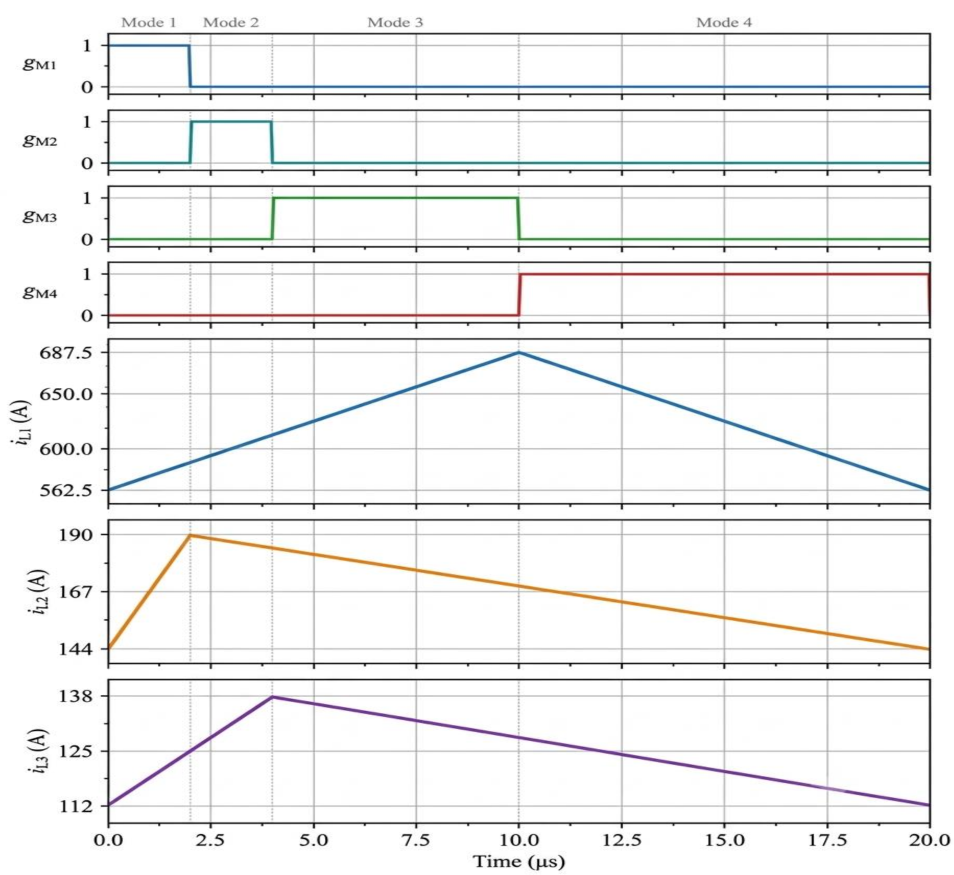

Fig. 2 Gate-pulse waveforms (M1-M4) and the corresponding inductor currents iL1, iL2, iL3 over one switching period, identifying the four sequential modes and their duty fractions

5.1. Mode 1: M1 ON (d1 = 0.10)

The 120-V bus charges all three inductors in parallel (D3, D4 reverse-biased):

$$v_{L1} = V_1 + V_3 = 120 \text{ V } \ (L_1 \text{ charging}) \tag{1}$$

$$v_{L2} = (V_1 + V_3) - v_{C4} = 108 \text{ V}, \quad v_{L3} = (V_1 + V_3) - v_{C5} = 96 \text{ V } \ (L_2, L_3 \text{ charging}) \tag{2}$$

so that

$$\frac{di_{L1}}{dt} = \frac{V_1 + V_3}{L_1}, \ \frac{di_{L2}}{dt} = \frac{(V_1 + V_3) - v_{C4}}{L_2}, \quad \frac{di_{L3}}{dt} = \frac{(V_1 + V_3) - v_{C5}}{L_3} \tag{3}$$

with iL1 ≈ 563-588 A, iL2 ≈ 144-190 A, iL3 ≈ 112-138 A (Figure 9), each inductor carrying its own branch current.

5.2. Mode 2: M2 ON (d2 = 0.10)

L1 and L3 continue charging while L2 freewheels through D3:

$$v_{L1} = V_1 + V_3 = 120 \text{ V } \ (L_1 \text{ charging}) \tag{4}$$

$$v_{L3} = (V_1 + V_3) - v_{C5} = 96 \text{ V } \ (L_3 \text{ charging}) \tag{5}$$

$$v_{L2} = -v_{C4} \approx -V_{R2} = -12 \text{ V } \ (L_2 \text{ freewheeling via } D_3) \tag{6}$$

and the freewheeling 12-V inductor obeys

$$\frac{di_{L2}}{dt} = -\frac{v_{C4}}{L_2} \tag{7}$$

5.3 Mode 3: M3 ON (d3 = 0.30)

Only L1 remains active along V1 → L1 → V3 → M3 → D1 → V1, accumulating the boost energy for Mode 4:

$$v_{L1} = V_1 + V_3 = 120 \text{ V} \tag{8}$$

$$v_{L2} = -V_{R2} = -12 \text{ V} \tag{9}$$

$$v_{L3} = -V_{R3} = -24 \text{ V} \tag{10}$$

$$i_{M3} = i_{D1} = i_{L1} \tag{11}$$

5.4 Mode 4: M4 ON (d4 = 0.50)

V2 and V3 in series feed the 800-V bus along V2 → L1 → V3 → D2 → M4 → R1/C3 → V2; since V2 + V3 = 680 V is below 800 V, L1 discharges at VR1 − (V2 + V3) = 120 V, balancing its 120-V × 0.5 Ts charge:

$$v_{L1} = (V_2 + V_3) - V_{R1} = 680 - 800 = -120 \text{ V} \tag{12}$$

$$v_{L2} = -V_{R2} = -12 \text{ V} \tag{13}$$

$$v_{L3} = -V_{R3} = -24 \text{ V} \tag{14}$$

$$i_{D2} = i_{M4} = i_{L1} \tag{15}$$

A closed loop exists in every interval (D1 return in Modes 1-3; D2 path in Mode 4), as the PLECS netlist enforces.

5.5. Volt-Second Balance Validation

For L1, charging equals discharging volt-seconds:

$$(V_1 + V_3)(d_1 + d_2 + d_3) = [V_{R1} - (V_2 + V_3)]\, d_4 \tag{16}$$

i.e., 120 × 0.50 = (800 − 680) × 0.50 (60 = 60).

The 12-V stage gives

$$[(V_1 + V_3) - V_{R2}]\, d_1 = V_{R2}\,(1 - d_1) \tag{17}$$

(108 × 0.10 = 12 × 0.90, 10.8 = 10.8) and the 24-V stage

$$[(V_1 + V_3) - V_{R3}](d_1 + d_2) = V_{R3}\,(1 - d_1 - d_2) \tag{18}$$

(96 × 0.20 = 24 × 0.80, 19.2 = 19.2), yielding VR1 = 800 V, VR2 = 12 V, VR3 = 24 V. Mode 2 (d2) decouples the 24-V balance from the 12-V rail; Mode 3 (d3) sustains the 800-V output.

6. Mathematical Modeling

6.1. State-Space Model

With x = [iL1, iL2, iL3, vC3, vC4, vC5]^T, u = [V1, V2, V3]^T, and y = [vR1, vR2, vR3]^T (C1, C2 treated as stiff), each mode k in {1,2,3,4} is linear time-invariant:

$$\frac{dx}{dt} = A_k x + B_k u \tag{19}$$

$$y = C_k x + D_k u \tag{20}$$

Mode 1 retains the full sixth order with three independent inductor-current states:

$$\frac{di_{L1}}{dt} = \frac{V_1 + V_3}{L_1}, \tag{21}$$

$$\frac{di_{L2}}{dt} = \frac{(V_1 + V_3) - v_{C4}}{L_2}, \frac{di_{L3}}{dt} = \frac{(V_1 + V_3) - v_{C5}}{L_3} \tag{22}$$

$$\frac{dv_{C3}}{dt} = -\frac{v_{C3}}{R_1 C_3} \tag{23}$$

$$\frac{dv_{C4}}{dt} = \frac{i_{L2}}{C_4} - \frac{v_{C4}}{R_2C_4}, \quad \frac{dv_{C5}}{dt} = \frac{i_{L3}}{C_5} - \frac{v_{C5}}{R_3C_5} \tag{24}$$

consistent with the independent triangular currents of Figure 9 (C3 discharges into R1 here, since L1 delivers only in Mode 4). Mode 2 is analogous with L2 freewheeling (diL2/dt = −vC4/L2); for Mode 4,

$$\frac{di_{L1}}{dt} = \frac{(V_2 + V_3) - v_{C3}}{L_1} \tag{25}$$

$$\frac{dv_{C3}}{dt} = \frac{i_{L1}}{C_3} - \frac{v_{C3}}{R_1C_3} \tag{26}$$

$$\frac{di_{L2}}{dt} = -\frac{v_{C4}}{L_2} \tag{27}$$

$$\frac{di_{L3}}{dt} = -\frac{v_{C5}}{L_3} \tag{28}$$

6.2. Averaged Model

Averaging over Ts with duty weights dk,

$$\frac{dx}{dt} = \sum_{k=1}^{4} d_k \ (A_k x + B_k u) \tag{29}$$

$$L_1 \frac{d\langle i_{L1}\rangle}{dt} = (V_1 + V_3)(d_1 + d_2 + d_3) + \ [(V_2 + V_3) - \langle v_{C3}\rangle]\, d_4 \tag{30}$$

$$L_2 \frac{d\langle i_{L2}\rangle}{dt} = [(V_1 + V_3) - \langle v_{C4}\rangle]\, d_1 - \ \langle v_{C4}\rangle\,(1 - d_1) \tag{31}$$

$$L_3 \frac{d\langle i_{L3}\rangle}{dt} = [(V_1 + V_3) - \langle v_{C5}\rangle](d_1 + d_2) - \ \langle v_{C5}\rangle\,(1 - d_1 - d_2) \tag{32}$$

$$C_3 \frac{d\langle v_{C3}\rangle}{dt} = \langle i_{L1}\rangle\, d_4 - \frac{\langle v_{C3}\rangle}{R_1} \tag{33}$$

$$C_4 \frac{d\langle v_{C4}\rangle}{dt} = \langle i_{L2}\rangle - \frac{\langle v_{C4}\rangle}{R_2} \tag{34}$$

$$C_5 \frac{d\langle v_{C5}\rangle}{dt} = \langle i_{L3}\rangle - \frac{\langle v_{C5}\rangle}{R_3} \tag{35}$$

Zero derivatives reproduce the Section 5.5 balances-vC3 = 800 V, vC4 = 12 V, vC5 = 24 V-and give iL1 = I_R1/d4 = 625 A, iL2 = 166.67 A, iL3 = 125 A (Figure 3).

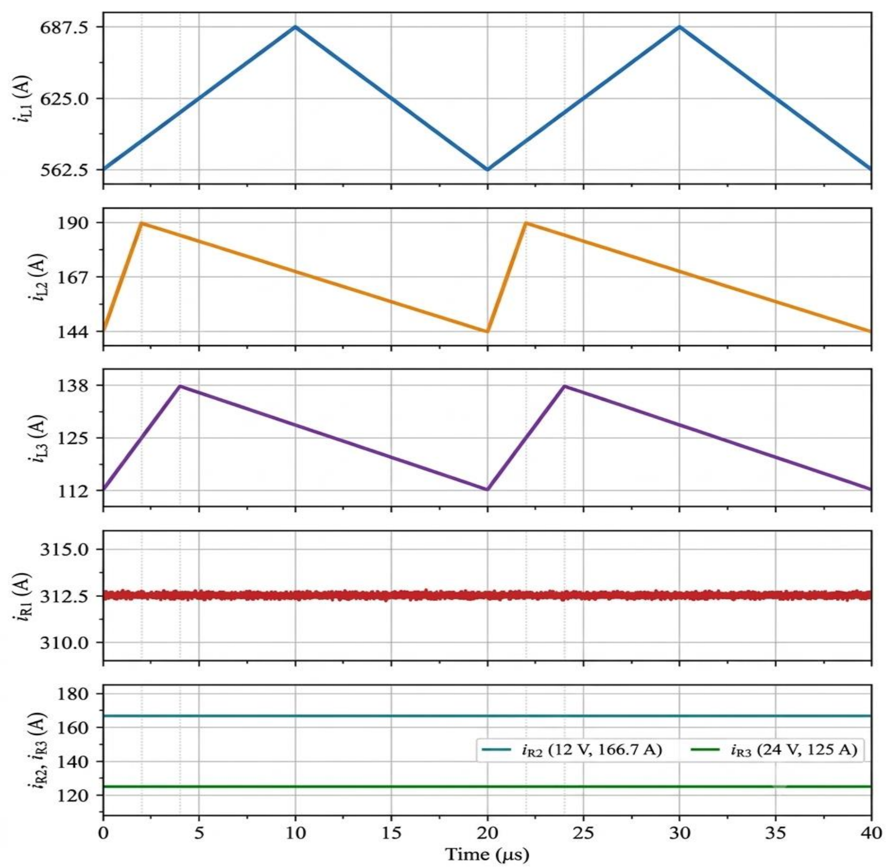

Fig. 3 Steady-state inductor and load currents (iL1, iL2, iL3, and the rail currents I_R1, I_R2, I_R3) illustrating the volt-second-balanced operation

6.3. Converter Gain Model

At steady state, the exact conversion ratios are

$$V_{R1} = (V_2 + V_3) + (V_1 + V_3)\,\frac{d_1 + d_2 + d_3}{d_4} \tag{36}$$

$$V_{R3} = (d_1 + d_2)(V_1 + V_3) \tag{37}$$

$$V_{R2} = d_1\,(V_1 + V_3) \tag{38}$$

i.e., VR1 = 800 V, VR3 = 24 V, VR2 = 12 V; the boost ratio is MR1 = 800/680 = 1.18 with buck ratios d1 = 0.10 and d1 + d2 = 0.20.

6.4. Power-Flow Model

With I_L1,avg = I_R1/d4 = 625 A (the general relation, not a fixed multiple of I_R1) and I_L1, pk = 687.5 A, charge balance gives the source currents:

$$I_{V1} = I_{L1,\text{avg}}\,(d_1 + d_2 + d_3) + I_{R2}\,d_1 + I_{R3}\,(d_1 + d_2) = 354.17\text{ A} \tag{39}$$

$$I_{V2} = I_{L1,\text{avg}}\,d_4 = 312.50\text{ A} \tag{40}$$

$$I_{V3} = I_{V1} + I_{V2} = 666.67\text{ A} \tag{41}$$

Hence P_V1 = 14.17 kW, P_V2 = 187.5 kW, P_V3 = 53.33 kW: 255.0 kW against the 250 + 2 + 3 = 255 kW load.

6.5. DTC Equations for the IPMSM

The stator flux is estimated in the α-β frame and the torque from the flux-current cross product, with the d-q form exposing the reluctance term:

$$\psi_\alpha = \int (v_\alpha - R_s i_\alpha)\,dt \tag{42}$$

$$\psi_\beta = \int (v_\beta - R_s i_\beta)\,dt \tag{43}$$

$$|\psi_s| = \sqrt{\psi_\alpha^2 + \psi_\beta^2} \tag{44}$$

$$\theta_\psi = \arctan\left(\frac{\psi_\beta}{\psi_\alpha}\right) \tag{45}$$

$$T_e = \frac{3}{2}\,p\,(\psi_\alpha i_\beta - \psi_\beta i_\alpha) \tag{46}$$

$$T_e = \frac{3}{2}\,p\,[\psi_f i_q + (L_d - L_q)\,i_d i_q] \tag{47}$$

Two-level hysteresis comparators with bands Hψ and HT process the errors:

$$H_\psi = +1 \text{ if } \left(|\psi_s^*| - |\psi_s|\right) > H_\psi - 1 \text{ if } < -H_\psi;\ 0 \text{ otherwise} \tag{48}$$

$$H_T = +1 \text{ if } (T_e^* - T_e) > H_T - 1 \text{ if } < -H_T;\ 0 \text{ otherwise} \tag{49}$$

6.6 SVM Equations

The sector N in {1,…,6} follows from θψ; two adjacent active vectors and the zero vectors are applied with dwell times.

$$T_1 = \frac{\sqrt{3}\,T_s}{V_{dc}}\left[\sin\left(\frac{N\pi}{3}\right) v_\alpha^* - \cos\left(\frac{N\pi}{3}\right) v_\beta^*\right] \tag{50}$$

$$T_2 = \frac{\sqrt{3}\,T_s}{V_{dc}}\left[-\sin\left(\frac{(N-1)\pi}{3}\right) v_\alpha^* + \cos\left(\frac{(N-1)\pi}{3}\right) v_\beta^*\right] \tag{51}$$

$$T_0 = T_s - T_1 - T_2 \tag{52}$$

and the symmetric seven-segment leg duties are

$$d_a = \frac{T_1 + T_2 + T_0/2}{T_s} \tag{53}$$

$$d_b = \frac{T_2 + T_0/2}{T_s} \tag{54}$$

$$d_c = \frac{T_0/2}{T_s} \tag{55}$$

With the T1/T2 assignment rotating by sector and Vdc, the regulated 800-V output of the proposed converter.

7. Component Design and Sizing Methodology

7.1. Inductor Design

Values use symbolic fsw, evaluated at an illustrative 50 kHz (Ts = 20 μs).

L1 is designed for CCM-peak ≈ 687.5 A versus ≈ 1250 A at boundary conduction, no DCM gain change at partial load, added damping of the L1-C3 resonance (Section 9.2):

$$L_{1,\text{crit}} = \frac{(V_1 + V_3)(d_1 + d_2 + d_3)^2}{2\,I_{R1}\,f_{sw}} = \frac{0.048}{f_{sw}} \tag{56}$$

$$L_{1,\text{CCM}} = \frac{(V_1 + V_3)(d_1 + d_2 + d_3)}{r_{\text{ripple}}\,I_{L1,\text{avg}}\,f_{sw}} = \frac{0.48}{f_{sw}} \tag{57}$$

giving L1,crit = 0.96 μH and the adopted L1 = 9.6 μH (ΔiL1 = 0.20 × 625 = 125 A; peak 687.5 A, valley 562.5 A, ≈ 45% below the boundary value). For L2 (I_R2 = 166.67 A, 2 kW, ΔiL2 = 50 A):

$$L_{2\text{ ripple}} = \frac{[(V_1 + V_3) - V_{R2}]\, d_1}{r_{\text{ripple}}\, I_{R2}\, f_{sw}} = \frac{0.216}{f_{sw}} \tag{58}$$

$$L_{2\text{ crit}} = \frac{V_{R2}\,(1 - d_1)}{2\, I_{R2}\, f_{sw}} = \frac{0.0324}{f_{sw}} \tag{59}$$

i.e., 4.32 μH and 0.648 μH, chosen L2 = 4.7 μH. For L3 (I_R3 = 125 A, 3 kW, ΔiL3 = 37.5 A):

$$L_{3,\text{ripple}} = \frac{[(V_1 + V_3) - V_{R3}](d_1 + d_2)}{r_{\text{ripple}}\, I_{R3}\, f_{sw}} = \frac{0.512}{f_{sw}} \tag{60}$$

$$L_{3,\text{crit}} = \frac{V_{R3}\,(1 - d_1 - d_2)}{2\, I_{R3}\, f_{sw}} = \frac{0.0768}{f_{sw}} \tag{61}$$

i.e., 10.24 μH and 1.54 μH, chosen L3 = 15 μH.

7.2. Capacitor Design

C3 supplies the load during (1 − d4); the buck capacitors follow C = ΔiL/(8 fsw Δv) at 1% voltage ripple:

$$C_3 = \frac{I_{R1}\,(1 - d_4)}{0.01\, V_{R1}\, f_{sw}} = \frac{19.53}{f_{sw}} \tag{62}$$

$$C_4 = \frac{\Delta i_{L2}}{8\, f_{sw} \cdot 0.01\, V_{R2}} = \frac{52.08}{f_{sw}} \tag{63}$$

$$C_5 = \frac{\Delta i_{L3}}{8\, f_{sw} \cdot 0.01\, V_{R3}} = \frac{19.53}{f_{sw}} \tag{64}$$

i.e., 390.6/1041.7/390.6 μF, chosen 470 μF / 1000 V, 1200 μF / 25 V, and 470 μF / 50 V. The input capacitors use 2% ripple with the average source currents-for the V1 loop, the correct numerator is the source current I_V1 = 354.17 A (not the traction-rail load current):

$$C_1 = \frac{I_{V1}\, d_1}{0.02\, V_1\, f_{sw}} = \frac{44.27}{f_{sw}} = 885.4\,\mu\text{F} \quad \text{(practical } 1000\,\mu\text{F} / 100\text{ V)} \tag{65}$$

$$C_2 = \frac{I_{V2}\, d_4}{0.02\, V_2\, f_{sw}} = \frac{13.02}{f_{sw}} = 260.4\,\mu\text{F} \quad \text{(practical } 330\,\mu\text{F} / 1000\text{ V)} \tag{66}$$

7.3. Semiconductor Stress Analysis

iL1 ramps from 562.5 A to 687.5 A across Modes 1-3 (587.5 A and 612.5 A at the ends of Modes 1 and 2) and decays back in Mode 4; D3/D4 carry the average rail currents:

$$V_{M1,\text{stress}} = V_{R1} = 800\text{ V} \tag{67}$$

$$V_{M2,\text{stress}} = V_1 + V_3 = 120\text{ V} \tag{68}$$

$$V_{M3,\text{stress}} = V_1 + V_3 = 120\text{ V} \tag{69}$$

$$V_{M4,\text{stress}} = V_{R1} = 800\text{ V} \tag{70}$$

Integrating the linear current segments over each conduction interval,

$$I_{M1,\text{avg}} = 1/2\ (562.5 + 587.5)\, d_1 = 57.5\text{ A},\quad I_{M1,\text{rms}} = 181.8\text{ A} \tag{71}$$

$$I_{M2,\text{avg}} = 1/2\ (587.5 + 612.5)\, d_2 = 60.0\text{ A},\quad I_{M2,\text{rms}} = 189.8\text{ A} \tag{72}$$

$$I_{M3,\text{avg}} = 1/2\ (612.5 + 687.5)\, d_3 = 195.0\text{ A},\quad I_{M3,\text{rms}} = 356.2\text{ A} \tag{73}$$

$$I_{M4,\text{avg}} = 1/2\ (687.5 + 562.5)\, d_4 = 312.5\text{ A},\quad I_{M4,\text{rms}} = 442.7\text{ A} \tag{74}$$

with peaks of 587.5, 612.5, 687.5, and 687.5 A; the four averages sum to 625 A = I_L1,avg, confirming iL1 always flows through exactly one switch.

7.4. Diode Stress Analysis

$$V_{D1,\text{rev}} = V_1 + V_3 = 120\text{ V} \tag{75}$$

$$V_{D2,\text{rev}} = V_{R1} = 800\text{ V} \tag{76}$$

$$V_{D3,\text{rev}} = V_{R2} = 12\text{ V} \tag{77}$$

$$V_{D4,\text{rev}} = V_{R3} = 24\text{ V} \tag{78}$$

D1 returns the loop current in Modes 1-3, and D2 conducts in Modes 1 and 4:

$$I_{D1,\text{avg}} = 1/2\ (562.5 + 687.5)(d_1 + d_2 + d_3) = 312.5\text{ A},\quad I_{D1,\text{rms}} = 442.7\text{ A} \tag{79}$$

$$I_{D2,\text{avg}} = 57.5\text{ (Mode 1)} + 312.5\text{ (Mode 4)} = 370.0\text{ A},\quad I_{D2,\text{rms}} = 478.6\text{ A} \tag{80}$$

$$I_{D3,\text{avg}} = I_{R2}\,(1 - d_1) = 166.67 \times 0.90 = 150.0\text{ A},\quad I_{D3,\text{rms}} = 158.1\text{ A} \tag{81}$$

$$I_{D4,\text{avg}} = I_{R3}\,(1 - d_1 - d_2) = 125 \times 0.80 = 100.0\text{ A},\quad I_{D4,\text{rms}} = 111.8\text{ A} \tag{82}$$

with peaks I_D1,pk = I_D2,pk = 687.5 A, I_D3,pk = 189.7 A, I_D4,pk = 137.8 A; the corrected I_D1,avg = 312.5 A is distinct from I_V1 = 354.17 A, which includes the auxiliary-rail contributions.

7.5. Design Summary Tables

Table 5. Inductor design summary (fsw = 50 kHz, illustrative)

Inductor	Critical (μH)	Ripple/CCM (μH)	Practical (μH)	Peak Current (A)
L1 (CCM)	0.96	9.6	9.6	687.5
L2 (CCM)	0.648	4.32	4.7	189.7
L3 (CCM)	1.54	10.24	15	137.8

Table 6. Capacitor design summary (fsw = 50 kHz, illustrative)

Capacitor	Calculated (μF)	Practical (μF / V)
C1	885.4	1000 / 100 V
C2	260.4	330 / 1000 V
C3	390.6	470 / 1000 V
C4	1041.7	1200 / 25 V
C5	390.6	470 / 50 V

Table 7. Semiconductor stress analysis (continuous conduction, boost-loop devices)

Device	Voltage Stress (V)	I_avg (A)	I_rms (A)	I_peak (A)
M1	800	57.5	181.8	587.5
M2	120	60.0	189.8	612.5
M3	120	195.0	356.2	687.5
M4	800	312.5	442.7	687.5
D1	120	312.5	442.7	687.5
D2	800	370.0	478.6	687.5
D3	12	150.0	158.1	189.7
D4	24	100.0	111.8	137.8

Tables 5 - 7 summarize the inductor and capacitor designs and the semiconductor stresses (the L2/L3 peaks listed are their rail-current ripple peaks).

7.6. Device Selection Guideline

M1/M4 block 800 V at 181.8/442.7 A rms, requiring 1200-V SiC MOSFETs (e.g., Wolfspeed C3M, ROHM SCT); M2/M3 block 120 V and use 200-V SiC parts, M3 paralleled (356.2 A rms, 687.5 A peak); D2 (≈ 800 V, 478.6 A rms) is a 1200-V SiC Schottky (or paralleled), with D3/D4 low-voltage Schottky diodes-a stepped voltage-class assignment essential for cost- and loss-effective implementation.

7.7. Loss Analysis and Efficiency Estimation

With Rds, on = 5 mΩ, diode Vf = 0.7 V and Rd ≈ 1 mΩ, and the Table 9 ESRs, the rated-point losses decompose as

$$P_{\text{cond},M} = \sum_k I_{Mk,\text{rms}}^2 \ R_{ds,on} = (181.8^2 + 189.8^2 + 356.2^2 + 442.7^2)(5 \times 10^{-3}) \approx 1960 \text{ W} \tag{83}$$

$$P_{\text{sw},M} = \sum_k f_{sw} \ \left(E_{on} + E_{off}\right)_k \approx 862 + 938 + 125 + 135 \approx 2060 \text{ W} \tag{84}$$

$$P_{\text{cond},D} = \sum_k I_{Dk,\text{avg}} \ V_f + \sum_k I_{Dk,\text{rms}}^2 \ R_d \approx 653 + 463 \approx 1115 \text{ W} \tag{85}$$

$$P_{Cu} = \sum_k I_{Lk,\text{rms}}^2 \ \text{ESR}_k \approx 196 + 56 + 31 \approx 283 \text{ W} \tag{86}$$

which, with an estimated ≈ 150-W core-loss budget, totals ≈ 5.57 kW for 255 kW delivered (250 kW traction + 5 kW auxiliary):

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{255000}{255000 + 5569} \approx 97.9\% \tag{87}$$

This converter-only figure reflects the lower RMS currents of CCM and excludes source resistances (as do the surveyed comparisons).

Including converter loss, the sources supply ≈ 260.6 kW; the Table 8 resistances give source-conduction losses of ≈ 0.63 + 0.98 + 2.22 ≈ 3.83 kW-dominated by the 666.7-A draw from V3, motivating a low-impedance interconnect-for ≈ 255/264.4 ≈ 96.4% system efficiency.

8. DTC-SVM Control Design

8.1. Torque and Flux Estimation

The outer loop sets torque/flux references, the inner DTC-SVM loop drives the inverter, and the energy-management unit (EMU) schedules d1-d4. The discrete flux estimator

$$\psi_{\alpha,\mathrm{raw}}(k) = \psi_{\alpha,\mathrm{raw}}(k-1) + T_s\,[v_\alpha(k) - R_s i_\alpha(k)] \quad (88)$$

$$\psi_{\beta,\mathrm{raw}}(k) = \psi_{\beta,\mathrm{raw}}(k-1) + T_s\,[v_\beta(k) - R_s i_\beta(k)] \quad (89)$$

accumulates a DC offset, removed by high-pass filtering the integrator output:

$$\hat{\psi}_s = H(s)\,\psi_{s,\mathrm{raw}},\quad H(s) = \frac{s}{s+\omega_c} \qquad \omega_c = 5\ \mathrm{rad/s}\ (\approx 0.8\ \mathrm{Hz}) \quad (90)$$

with the ≈ 0.8-Hz cutoff well below the 66.7-Hz minimum fundamental (1000 r/min); backward-Euler discretization with β ≈ 0.9995 at Ts,ctrl = 100 µs gives

$$\hat{\psi}_s(k) = \beta\left[\hat{\psi}_s(k-1) + \psi_{s,\mathrm{raw}}(k) - \psi_{s,\mathrm{raw}}(k-1)\right] \quad (91)$$

The standard voltage-model drift remedy [47]; torque follows from (46) each cycle.

8.2. Hysteresis Controllers

Hψ = ±0.5% of the 0.33-Wb MTPA flux ≈ ±1.65 mWb and HT = ±2% of 400 N·m = ±8 N·m:

$$d_\psi = H_\psi\left(\psi_s^* - \psi_s\right) \quad (92)$$

$$d_T = H_T\left(T_e^* - T_e\right) \quad (93)$$

with dψ, dT ∈ {−1, 0, +1} feeding the vector selection.

8.3. Sector Identification and Reference Vector

The flux plane divides into six 60° sectors:

$$N = \mathrm{floor}\left[\frac{\theta_\psi + \pi/6}{\pi/3}\right] + 1,\quad N \in \{1, \dots, 6\} \quad (94)$$

The classical switching table is replaced by a direct reference-vector calculator,

$$v_\alpha^* = \frac{\psi_s^* \cos\theta_\psi^* - \psi_s \cos\theta_\psi}{T_s} + R_s i_\alpha \quad (95)$$

$$v_\beta^* = \frac{\psi_s^* \sin\theta_\psi^* - \psi_s \sin\theta_\psi}{T_s} + R_s i_\beta \quad (96)$$

and with Te ≈ (3/2) p ψf iq, i_q = |ψs| sin(Δθψ)/Lq, the torque loop commands the (dimensionless-argument) load-angle increment

$$\Delta\theta_\psi = \arcsin\left[\frac{2\,L_q\,\Delta T_e}{3\,p\,\psi_f\,|\psi_s|}\right] \quad (97)$$

limited to the linear modulation range.

8.4. SVM Generation and Duty-Cycle Synthesis

The dwell times (50)-(52) and the symmetric seven-segment sequence {V0, Vk, Vk+1, V7, Vk+1, Vk, V0} minimize ripple and switching loss; the leg duties (53)-(55) are clamped to [0, 1] and loaded into the PWM registers.

8.5. Power-Sharing Equations and Cascade Architecture

With the Section 6.4 powers, the sharing ratios are k1 = 0.056, k2 = 0.735, k3 = 0.209, and PI laws update the duties:

$$d_1(k+1) = d_1(k) + K_{p1}\left(V_{R2}^* - V_{R2}\right) + K_{i1}\int\left(V_{R2}^* - V_{R2}\right)dt \quad (98)$$

$$d_2(k+1) = d_2(k) + K_{p2}\left(V_{R3}^* - V_{R3}\right) + K_{i2}\int\left(V_{R3}^* - V_{R3}\right)dt - \gamma\,d_1(k+1) \quad (99)$$

$$d_4(k+1) = d_4(k) + K_{p4}\left(V_{R1}^* - V_{R1}\right) + K_{i4}\int\left(V_{R1}^* - V_{R1}\right)dt \quad (100)$$

$$d_3(k+1) = 1 - d_1(k+1) - d_2(k+1) - d_4(k+1) \quad (101)$$

Where γ decouples the shared d1 term in the 24-V ratio and (101) enforces Σd = 1. The two controllers form a cascade, not a co-designed unit: DTC-SVM regulates the inverter, the EMU regulates the converter through (98)-(101), and the only coupling is the shared DC-link voltage-load steps on any rail are disturbances rejected by the respective loops, as the paper's title reflects.

8.6. Torque-Ripple, Flux-Ripple, and THD Reduction

Continuous vector synthesis bounds the torque ripple to approximately.

$$\Delta T_e \approx \frac{3}{2}\,p\,|\psi_s|\,|v_s - e_s|\,\frac{T_s}{L_q} \quad (102)$$

three to five times below classical DTC; the near-circular flux locus holds ≈ 3.3-mWb ripple (1% of 0.33 Wb) versus 10-17 mWb, and THD falls from 5-8% to 2-3%.

9. Stability Analysis

9.1. Lyapunov Stability of DTC-SVM

With errors eψ = ψs* − ψs and eT = Te* − Te,

$$V(e_\psi, e_T) = 1/2\ e_\psi^2 + 1/2\ e_T^2 \quad (103)$$

$$\frac{dV}{dt} = e_\psi \cdot \frac{de_\psi}{dt} + e_T \cdot \frac{de_T}{dt} \quad (104)$$

$$\frac{de_\psi}{dt} = -\left(v_\psi - R_s i_\psi\right) \quad (105)$$

Where vψ, iψ are the radial components. Differentiating the torque (46) and substituting dψ/dt = v − Rs i,

$$\frac{dT_e}{dt} = \frac{3}{2}\, p\, [\, (v_\alpha - R_s i_\alpha)\, i_\beta - \left(v_\beta - R_s i_\beta\right) i_\alpha + \psi_\alpha \frac{di_\beta}{dt} - \psi_\beta \frac{di_\alpha}{dt}\,] \quad (106)$$

and in the dominant-term (large-saliency) approximation

$$\frac{dT_e}{dt} \approx \frac{3}{2}\frac{p}{L_q}\left(\psi_\alpha v_\beta - \psi_\beta v_\alpha\right) - \frac{3}{2}\frac{p}{L_q}\ \omega_r\, \psi_f^2 \quad (107)$$

So the torque rate follows the tangential voltage; hence.

$$\frac{de_T}{dt} = \frac{dT_e^*}{dt} - \frac{3}{2}\frac{p}{L_q}\left(\psi_\alpha v_\beta - \psi_\beta v_\alpha\right) + \frac{3}{2}\frac{p}{L_q}\ \omega_r\, \psi_f^2 \quad (108)$$

The DTC-SVM law makes both error products negative, and with the inverter voltage bounded, the derivative is negative outside a small residual set:

$$\frac{dV}{dt} \le -\lambda\left(e_\psi^2 + e_T^2\right) = -2\lambda V \quad (109)$$
(V outside the residual set)

-practical asymptotic stability with ultimately bounded errors. The rate is derived:

$$\left.\frac{dT_e}{dt}\right|_{\max} = \frac{3}{2}\frac{p\,\psi_f\left(v_{q,\max} - e_s\right)}{L_q} \quad (110)$$

with vq,max = Vdc/√3 ≈ 462 V and es = ωe|ψs| ≈ 138 V at 1000 r/min gives ≈ 2.4×10⁵ N·m/s (the 400-N·m step in ≈ 1.7 ms), and the bandwidth

$$\lambda = \omega_{c,cl} \approx \frac{4.605}{t_s} \approx \frac{4.605}{4\ \text{ms}} \approx 1.2 \times 10^3\ \text{s}^{-1} \quad (111)$$

i.e., ≈ 4-ms settling to a 1% band, consistent with the ≈ 2-ms rise; global exponential stability is not claimed for the switching, input-bounded system.

9.2. Small-Signal Converter Model and Eigenvalue Analysis

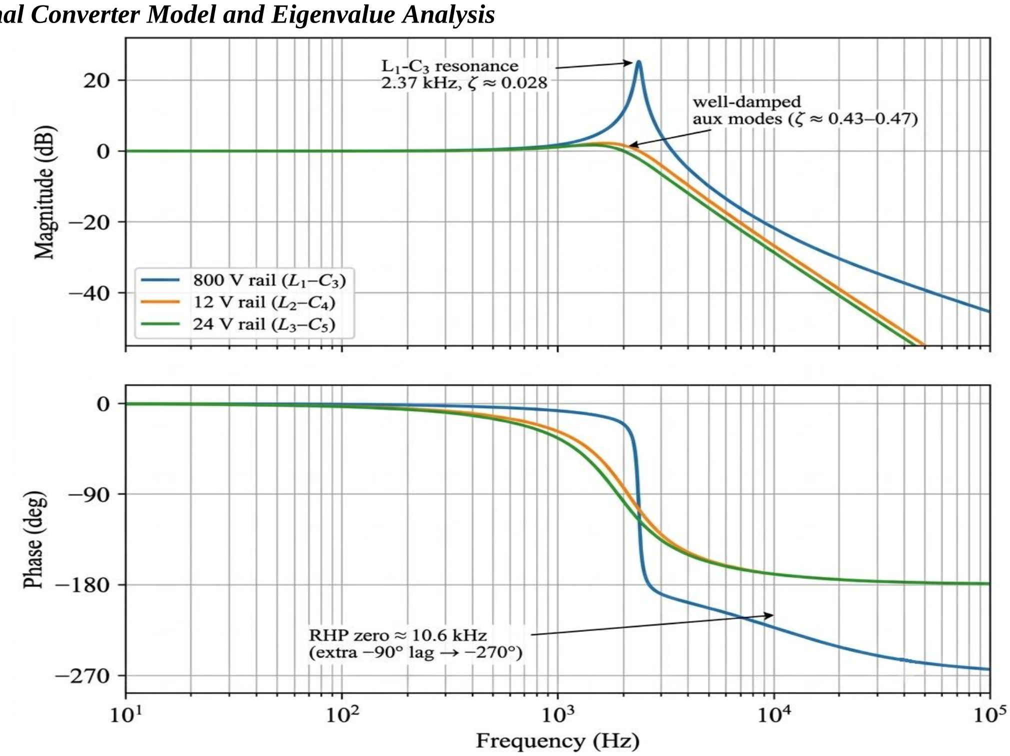

Fig. 4 Bode plots of the linearized closed-loop system (control-to-output transfer functions of the three rails), confirming the stable, lightly damped L1-C3 mode and the well-damped auxiliary modes

Linearizing the averaged model (29)-(35) about the operating point,

$$\frac{d\tilde{\imath}}{dt} = A\,\tilde{\imath} + B\,\tilde{u} \tag{112}$$

$$\tilde{y} = C\,\tilde{\imath} + D\,\tilde{u} \tag{113}$$

with ì = [ĩL1, ĩL2, ĩL3, ṽC3, ṽC4, ṽC5]ᵀ and ŭ = [d̃1, d̃2, d̃4]ᵀ. With the Section 7 values and R1 = 2.56 Ω, R2 = 0.072 Ω, R3 = 0.192 Ω, det(λI − A) = 0 yields

$$\lambda_{1,2} = -4.16 \times 10^2 \pm j\,1.488 \times 10^4 \quad (L_1\text{-}C_3 \text{ mode, } f_d \approx 2.37 \text{ kHz, } \zeta \approx 0.028) \tag{114}$$

$$\lambda_{3,4} = -5.79 \times 10^3 \pm j\,1.199 \times 10^4 \quad (L_2\text{-}C_4 \text{ mode, } f_d \approx 1.91 \text{ kHz, } \zeta \approx 0.43) \tag{115}$$

$$\lambda_{5,6} = -5.54 \times 10^3 \pm j\,1.054 \times 10^4 \quad (L_3\text{-}C_5 \text{ mode, } f_d \approx 1.68 \text{ kHz, } \zeta \approx 0.47) \tag{116}$$

All poles are in the open left-half plane; the buck modes are well damped (ζ ≈ 0.43-0.47) and the lightly damped L1-C3 mode (ζ ≈ 0.028)-three times better damped than a boundary design-is stabilized by the regulator (100) and component ESR, with all resonances (1.68-2.37 kHz) far below 50 kHz. The boost rail carries an RHP zero ωRHPZ ≈ $R1(1 - D)^2/L1 \approx 6.7\times10^4$ rad/s (≈ 10.6 kHz at D = 0.5), limiting the 800-V crossover to ≈ 1-3 kHz; the control-to-output responses are shown in Figure 4.

9.3. Convergence and Boundedness Analysis

By input-to-state stability of the cascade, bounded converging rail voltages keep the machine states bounded; vC3 is passively limited by the boost stage and vC4, vC5 by their buck ratios, so the system is BIBO stable.

10. PLECS Simulation Framework

No hardware prototype, experimental verification, laboratory testing, PCB implementation, thermal-camera measurement, oscilloscope capture, or real-time implementation is claimed; all results use a fixed-step 100-ns (a sub-multiple of the 20-µs converter and 100-µs control periods) with ideal switches and the parameters of Tables 8 - 10-identical to the eigenvalue analysis. The 5-mΩ resistance of V3, which carries ≈ 667 A in every mode, dominates the source-side losses of Section 7.7; the machine parameters are those of Table 4.

Table 8. Source parameters

Source	Voltage (V)	Internal Resistance (mΩ)
V1 (Auxiliary Battery)	40	5
V2 (Traction Battery)	600	10
V3 (Shared Battery)	80	5

Table 9. Converter parameters

Component	Value	ESR / Rds,on
L1	9.6 µH	0.5 mΩ
L2	4.7 µH	2.0 mΩ
L3	15 µH	2.0 mΩ
C1	1000 µF	10 mΩ
C2	330 µF	10 mΩ
C3	470 µF	15 mΩ
C4	1200 µF	5 mΩ
C5	470 µF	10 mΩ
M1-M4	SiC MOSFET	Rds,on = 5 mΩ
D1-D4	SiC Schottky	Vf = 0.7 V

Table 10. Controller parameters

Parameter	Value	Description
Ts,conv	20 µs	Converter switching period (50 kHz)
Ts,ctrl	100 µs	DTC-SVM control/inverter period (10 kHz)
Hψ	±1.65 mWb	Flux hysteresis band (0.5% of 0.33 Wb)
HT	±8 N·m	Torque hysteresis band (2% of 400 N·m)
Kp1, Ki1	0.05, 50	12-V rail PI gains
Kp2, Ki2	0.04, 40	24-V rail PI gains
Kp4, Ki4	0.02, 20	800-V rail PI gains

11. Results and Discussion

11.1. Torque Response

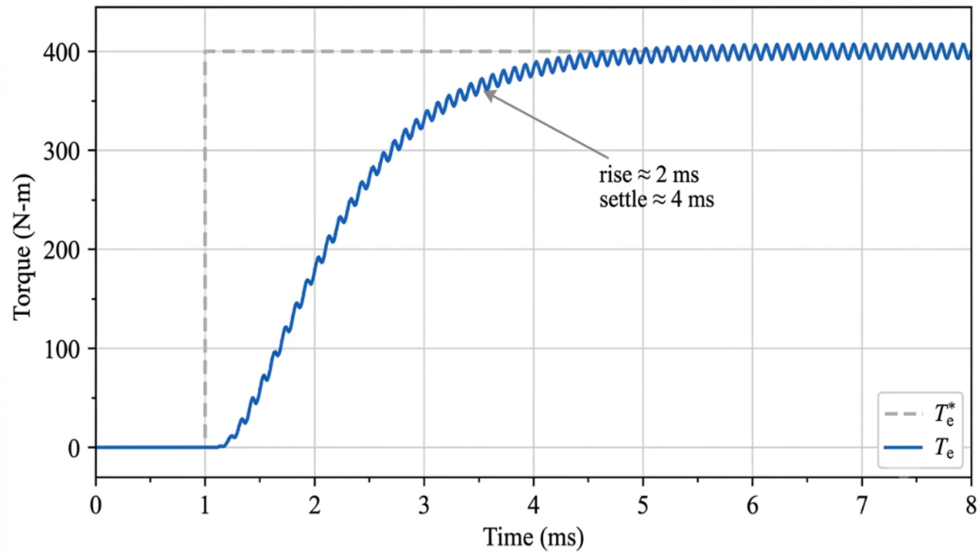

Fig. 5 Torque response to a 0-to-400-N·m step command at 1000 r/min

As Figure 5 shows, torque rises in ≈ 2 ms and settles within 4 ms-matching the Lyapunov rate of (109)-(111)-with no overshoot, ±6-N·m ripple (≈ 1.5%, 3-4× below classical DTC), a 0.1-ms SVM/PWM delay, and a slope agreeing with the ≈ 1.7-ms slew of (110); the dominant ripple sits at the 10-kHz SVM frequency, confirming constant-frequency operation essential for tip-in drivability.

11.2. Flux Response

In Figure 6, the flux stays within ±1% of the 0.33-Wb reference, dipping ≈ 0.8% at the torque step and recovering within 3 ms-torque-flux decoupling in action; the α-β locus is near-circular with ≈ 3.3-mWb (1%) ripple versus 10-17 mWb for classical DTC, protecting the magnets and MTPA efficiency.

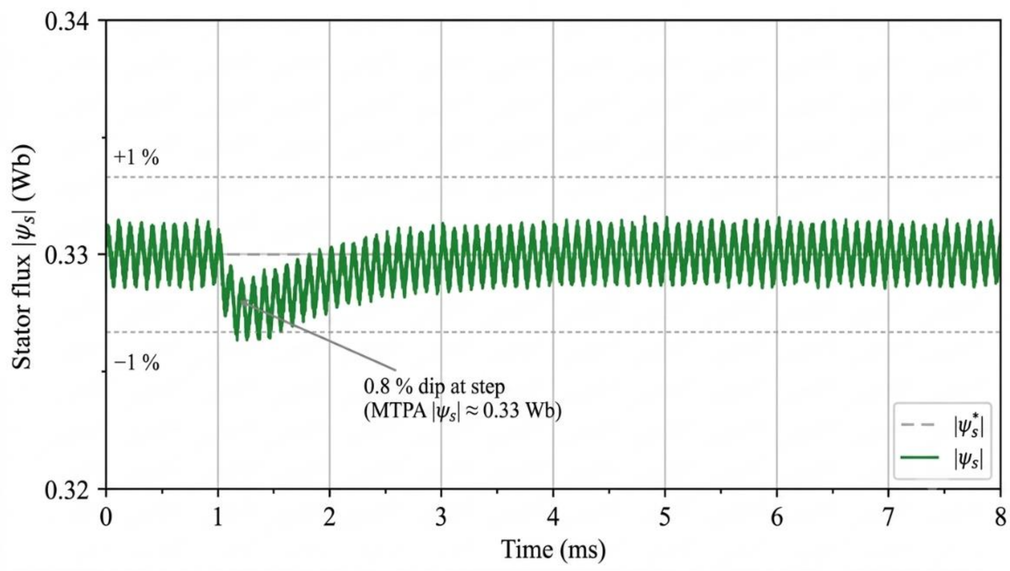

Fig. 6 Stator-flux magnitude response during the torque step

11.3. Speed Response

The reversal of Figure 7 shows ≈ 160 - ms near-linear ramps (J·Δω/Te = 0.05 × 1257 / 400) with ≈ 120-r/min (≈ 2%) peak tracking error and anti-windup-confirmed saturation at the 400 - N·m limit; the drive runs MTPA below the ≈ 3300 - r/min base speed, field-weakens to 6000 r/min within the 462 - V limit, and extends constant power to 18000 r/min (3:1 CPSR), with ≈ ±5-r/min (0.08%) steady ripple and the MTPA-to-field-weakening transition scheduled by ψs*(ωr).

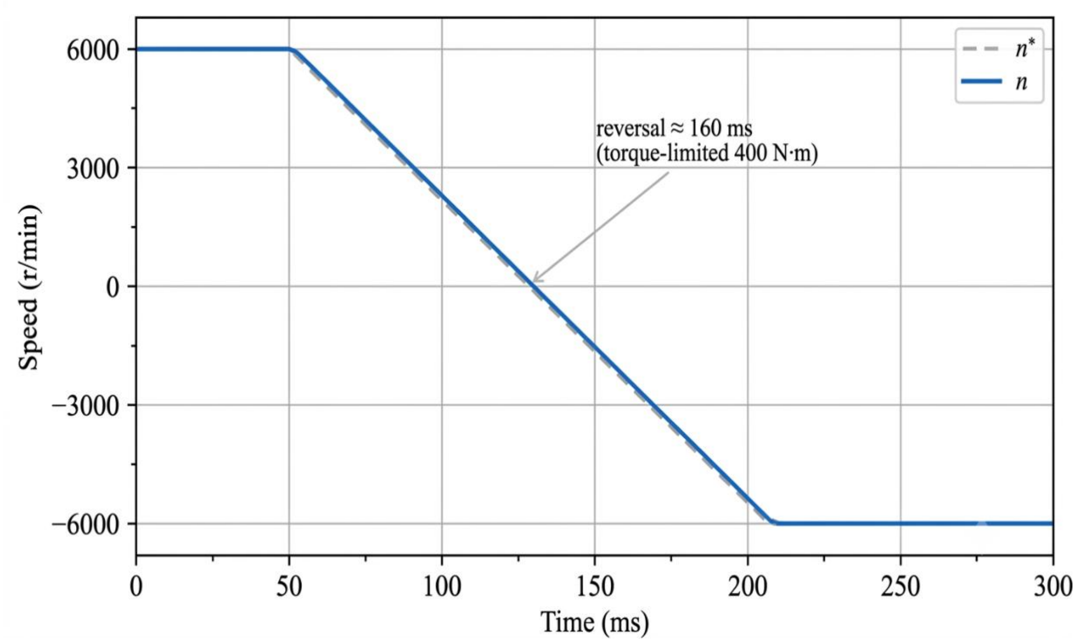

Fig. 7 Speed reversal from +6000 r/min to −6000 r/min

11.4. Harmonic Spectrum

In the spectrum of Figure 8 the 200-Hz fundamental (4 pole pairs × 3000/60 rev/s) carries ≈ 215 A rms at 2.4% THD, with the 5th/7th harmonics at ≈ −42/−45 dB; transient low-frequency content decays within ≈ 10 ms, and 10-kHz clusters stay below −60 dB-the 2-μs dead time leaving small 5th/7th residues-meeting IEEE 519 and IEC 61800-3 for onboard compatibility.

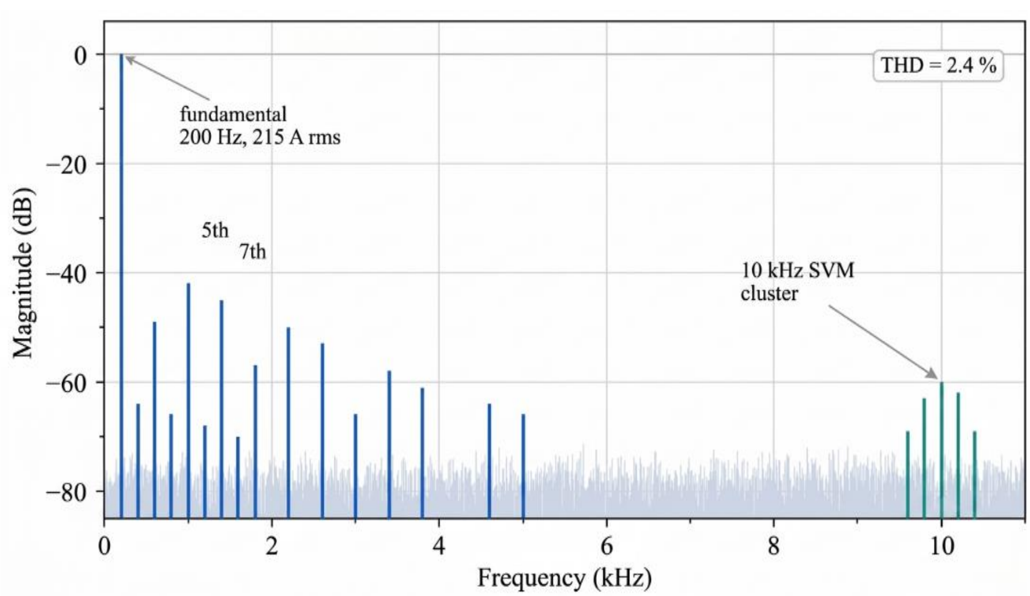

Fig. 8 Phase-current harmonic spectrum at rated torque and 3000 r/min.

11.5. Converter Waveforms

In Figure 9, iL1 ramps 562.5-687.5 A about its 625-A average (20% ripple, CCM confirmed) while iL2/iL3 carry independent 46-A and 26-A triangles about 166.67 A and 125 A; load-step responses follow $\tau L2 = L2/R2 \approx 65$ μs and $\tau L3 = L3/R3 \approx 78$ μs with L1 settling within a few periods, all waveforms periodic at Ts = 20 μs and peaks within 2% of the Section 7 design. During the load step (Figure 10), the 800-V, 24-V, and 12-V rails dip ≈ 4 V (0.5%), ≈ 0.3 V (≈ 1.25%), and ≈ 0.15 V (≈ 1.25%), recovering in 200, 150, and 120 μs, with cross-regulation bounded by the independent d2 trim-vital for ECUs, lighting, and HVAC.

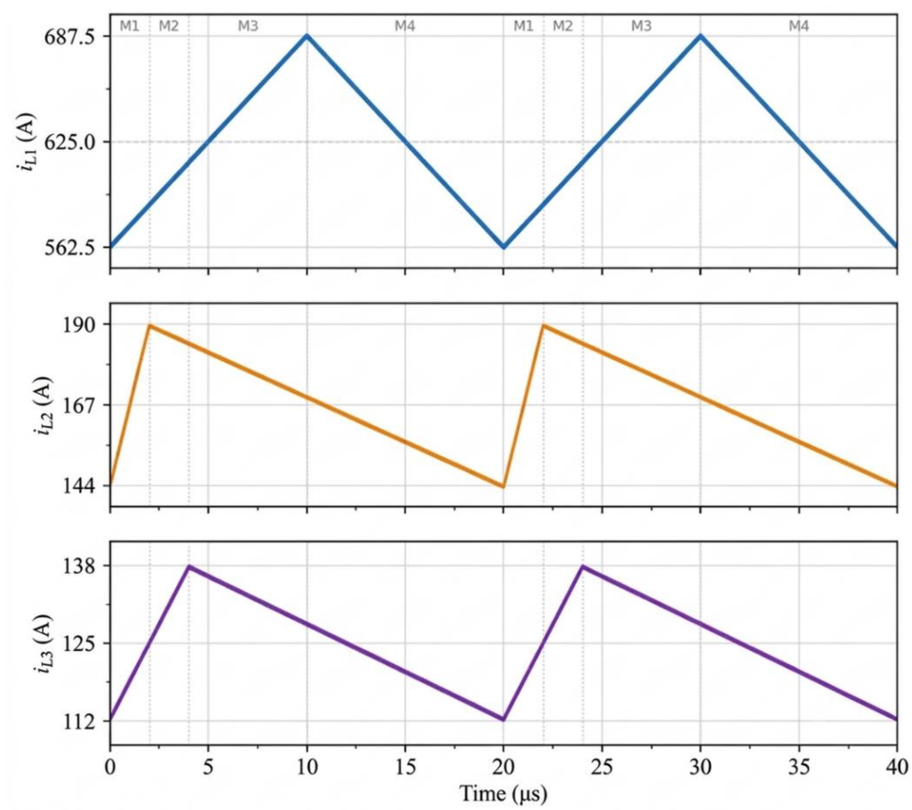

Fig. 9 Inductor currents iL1, iL2, iL3 over two switching periods (steady state)

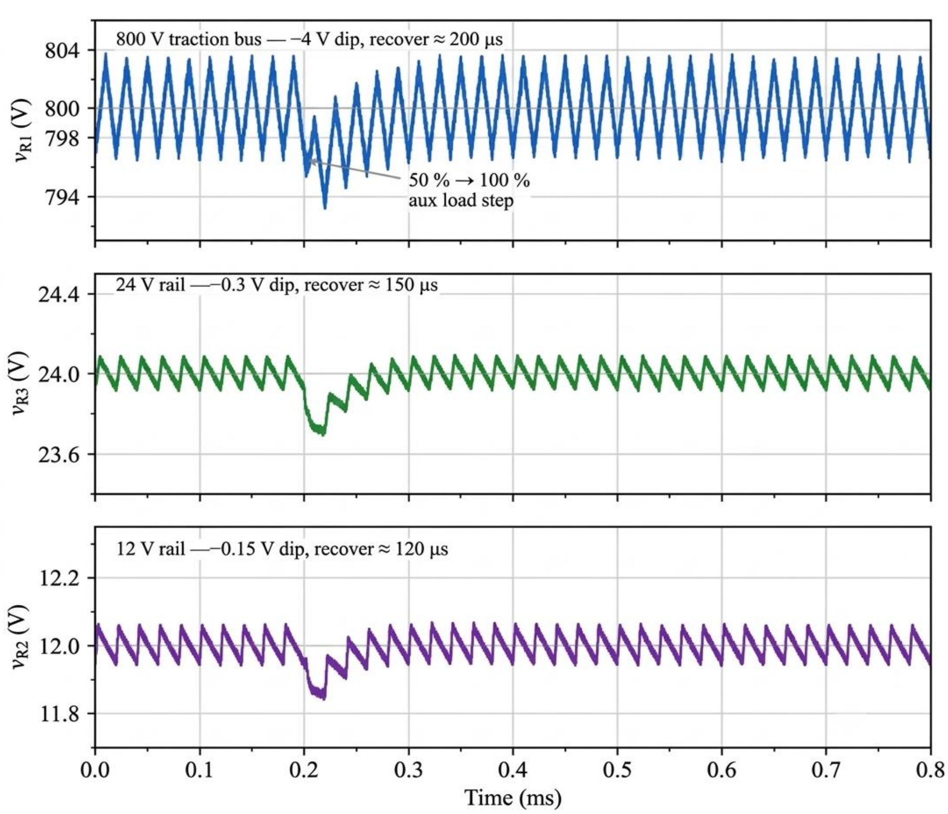

Fig. 10 Output voltages vR1, vR2, vR3 during a 50%-100% auxiliary load step

11.6. Switching-Frequency Spectrum

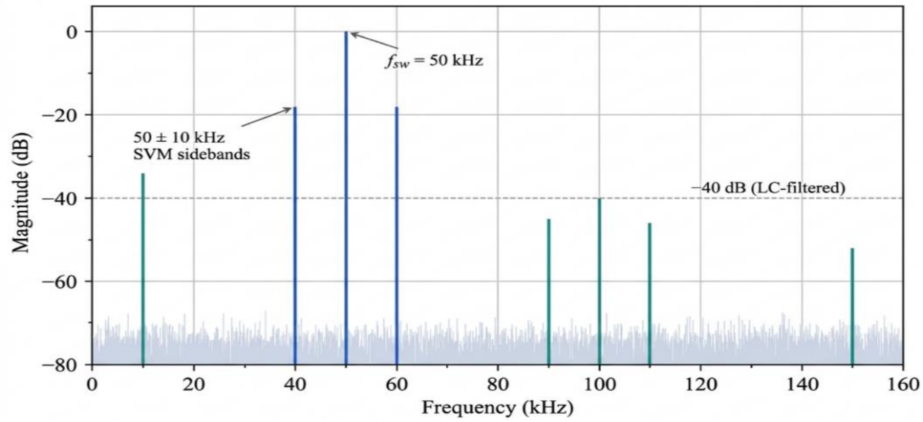

Fig. 11 Converter output-voltage spectrum showing SVM sidebands

The spectrum of Figure 11 shows the 50-kHz converter line with 50 ± 10-kHz DTC-SVM sidebands and content above 100 kHz attenuated below −40 dB by the output LC filters, simplifying EMI design toward CISPR 25 compliance.

12. Comparative Analysis

Benchmarked in Table 1 (Section 2), the proposed system uniquely delivers three outputs (800, 24, 12 V) from three heterogeneous inputs: [11] offers three outputs from one input without a high-voltage rail, and [16, 23, 26, 40] reach high gain for one output only. DTC-SVM-unreported for a MIMO-fed IPMSM in the surveyed literature-provides constant frequency and 2.4% THD versus the PWM methods of [5, 10, 44], and the 97.9% analytical peak efficiency (Section 7.7) exceeds [11] (96.5%) and [26] (96.0%) with fewer devices than isolated counterparts; the comparison is indicative, prior figures reflecting their own conditions.

As Figure 12 shows, efficiency peaks near 97.9% close to rated load, MOSFET conduction and switching losses dominating-motivating SiC and the interleaving suggested as future work.

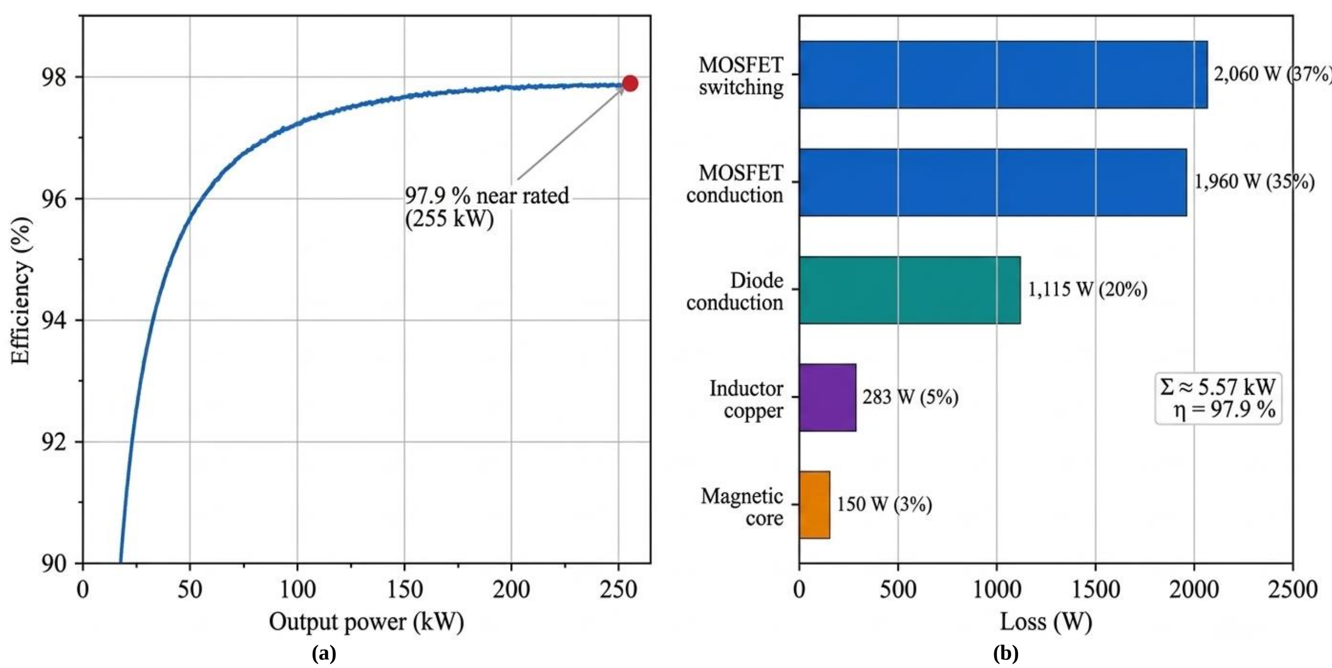

Fig. 12 Analytical efficiency versus output power for the proposed converter, indicating the 97.9% peak near rated load and the loss-component breakdown of Section 7.7

The surveyed work solves parts of this problem separately. Isolated multiport stages built on dual- and triple-active bridges [36, 45] provide galvanic isolation but carry a transformer, with the weight, volume, and core loss that implies (Table 3), and the modular charger converters [24, 25] address off-board charging rather than onboard rail generation. The non-isolated multi-input converters [5, 16, 23, 26-28, 33, 41, 43] obtain high gain or reduced stress for one regulated output, and the renewable-oriented interfaces [1, 15, 17, 18, 30-32, 34, 38, 39, 42] regulate one output or low-voltage buses only. Among the EV-oriented converters, [10] derives two outputs from three inputs through shared magnetics, [6] feeds an induction-motor drive from a multi-input single-output stage, [7] covers the 12-V/48-V auxiliary domain, and [11] produces three outputs from a single input without a high-voltage rail. On the control side, DTC [46] and its sensorless form [47] treat the inverter-fed machine alone, while the sliding-mode [3], adaptive [29], and NSGA-II co-optimized [12, 37] schemes act on the converter side; no surveyed paper analyzes a MIMO converter and the DTC-SVM traction drive it feeds as one cascade.

Three features separate the proposed converter from this corpus. First, one boost inductor L1 is time-shared between two source stacks that have V3 in common: the 120-V stack (V1 + V3) charges L1 during d1 + d2 + d3 and the 680-V stack (V2 + V3) discharges it into the 800-V rail during d4, so the traction rail follows from the four-switch schedule of Section 5 and the volt-second balance (16) without the coupled inductors of [40], the switched-capacitor cells of [33, 41], or the transformer of [36, 45]. Second, the 12-V and 24-V rails are drawn from the same 120-V stack by buck action through L2 and L3 with their own freewheel diodes D3 and D4, so the three inductor currents are independent (Figure 9) while the duties d1 and d1 + d2, with d2 as the 24-V trim (Sections 4, 5.5), are decoupled by γ in (99); this is what lets one stage regulate an 800-V rail and two low-voltage rails at once, which no Table 1 entry does. Third, the converter is not analyzed on its own: the DTC-SVM drive is designed for the 250-kW IPMSM of Table 4, the two form a cascade coupled only through the regulated 800-V link (Section 8.5), and that cascade is examined by the Lyapunov, eigenvalue, and input-to-state arguments of Section 9 with the sizing of Section 7 and the parameters of Tables 8 - 10, whereas [12, 37] optimize converter and controller numerically, [29] regulates a magnetically coupled multiport, and [46, 47] treat the machine alone. This analytical cascade treatment of a MIMO-fed IPMSM drive is the contribution claimed.

Against the Table 1 data, the proposed system is better in three respects and not in two. (i) It is the only entry regulating three outputs from three inputs; [10] reaches two outputs and [11] three outputs from one input. (ii) The analytical converter-only efficiency of 97.9% at the 255-kW rated point (87) is 1.4 percentage points above [11] (96.5%), 1.9 above [26] (96.0%), 2.4 above [23] (95.5%), and 2.6-4.4 above the remaining entries (93.5-95.3%). (iii) The 2.4% phase-current THD of Figure 8 is below the 2.5-3.8% of [5, 10, 16, 17, 23, 28, 33, 40, 44] but not below [26] (2.2%) or [11] (2.0%); for the drive itself the relevant reference is classical DTC (Table 2), against which the torque ripple of Figure 5 (±6 N·m, ≈ 1.5%) is 3-4 times lower and the flux ripple of Figure 6 (≈ 3.3 mWb) compares with 10-17 mWb. On voltage gain, the converter is not superior-its traction rail needs a boost ratio of only 1.18 (Section 6.3), whereas [16, 28, 40] are built for very high step-up-and on isolation, it is inferior to [36, 45]. As noted in Section 2, the prior values are those reported by their authors under their own conditions, so the efficiency and THD margins are indicative; the following paragraphs explain why the proposed values are obtained, not that they have been measured.

The efficiency value is the outcome of the loss decomposition (83)-(87) shown in Figure 12 (b), and three design features set the size of its terms. First, source stacking: V2 + V3 = 680 V already supplies most of the 800-V rail, so L1 has to balance only 120 V × 0.5 Ts per period (16), and in Mode 4 the traction power passes through one inductor, one diode, and one MOSFET (V2 → L1 → V3 → D2 → M4 → R1) with no transformer, coupled winding, or switched-capacitor stage in the path; the magnetic loss is therefore confined to the ≈ 283-W copper and ≈ 150-W core terms, 8% of the budget in Figure 12 (b), whereas the coupled-winding [40] and switched-capacitor [33] entries, at 93.5% and 94.2% in Table 1, carry such extra elements in their power path. Second, CCM sizing: L1 = 9.6 μH is ten times the critical value of (56), so the ripple is 20% of the 625-A average and the peak is 687.5 A instead of ≈ 1250 A at boundary conduction (Section 7.1); with the boost-loop current confined to 562.5-687.5 A (Section 7.3), the RMS currents entering (83), (85), and (86) stay close to the minimum the average currents allow-the CCM effect noted in Section 7.7. Third, stepped voltage classes: only M1, M4, and D2 block 800 V while M2, M3, and D1 block 120 V (67)-(70), (75), (76), which permits the 200-V/1200-V SiC assignment of Section 7.6 with the Rds, on = 5 mΩ and Vf = 0.7 V used in (83)-(85). Even so, MOSFET conduction (≈ 1960 W) and switching (≈ 2060 W) are 72% of the ≈ 5.57-kW total, which is why soft switching and interleaving of L1 remain future work, and the ≈ 96.4% system efficiency with source resistances (Section 7.7), dominated by the ≈ 667-A draw from V3 in every mode, is reported so that 97.9% is not read as a vehicle-level figure.

The drive-side figures have an equally specific origin. Classical DTC applies one discrete inverter vector per control cycle from a hysteresis switching table, so its switching frequency, torque ripple, and current harmonics change with the operating point; the DTC-SVM of Section 8 keeps the comparators (92), (93) only as error quantizers and replaces the table by the reference-vector calculator (95)-(97) and the seven-segment SVM (50)-(55), so a voltage vector of any magnitude and angle within the linear range is synthesized every Ts, ctrl = 100 μs. The consequences are those of Section 11: the torque ripple is bounded by (102) to ±6 N·m (Figure 5), the flux locus stays within 1% of 0.33 Wb (Figure 6), and the harmonic content is concentrated at the fixed 10-kHz frequency and its sidebands (Figure 8, Figure 11) instead of being spread over a variable band, which is why the phase-current THD is 2.4% against the 5-8% of classical DTC (Section 8.6). The ≈ 2-ms torque rise is set by the voltage headroom of the regulated 800-V link-vq, max ≈ 462 V against es ≈ 138 V at 1000 r/min in (110)-which the boost rail provides (Section 3). On the converter side, the separate inductors and freewheel diodes of the auxiliary rails, with the d2 trim and the γ term of (99), hold the cross-regulation during the 50%-100% auxiliary load step to ≈ 0.5% on the 800-V rail and ≈ 1.25% on the 12-V and 24-V rails with 120-200-µs recovery (Figure 10), a separation that the shared-magnetics [10] and single-output [5, 16, 23, 26] converters do not provide; Table 1 lists no cross-regulation figure for them and none is inferred. The price of these mechanisms is also stated: no galvanic isolation (Section 4), three separate inductors, and a shared source that conducts in every mode and dominates the source-side loss (Section 7.7).

13. Conclusion

A non-isolated three-input three-output converter integrated with a DTC-SVM IPMSM drive has been analyzed. The four-mode KVL-analyzed schedule (d1 = 0.10, d2 = 0.10, d3 = 0.30, d4 = 0.50) satisfies exact volt-second balance, the source powers (14.17, 187.5, 53.33 kW) totalling the 255-kW demand; CCM sizing gives L1 = 9.6 µH (687.5-A peak), L2/L3 rail ripple peaks near 190/138 A, 1200-V/200-V SiC device classes from the stress analysis, and a 97.9% analytical peak efficiency from the explicit loss decomposition. The drive achieves ≈ 2-ms torque rise, ≈ ±1.5% torque ripple, and ≈ 2.4% THD at constant switching frequency, with $\lambda \approx 1.2\times10^3\ s^{-1}$ practical asymptotic stability, all-left-half-plane converter eigenvalues, and a regulator-damped boost mode; converter and drive form a cascade coupled only through the DC link, and the PLECS framework provides reproducible, hardware-independent evaluation. Being non-isolated, the topology remains an academic feasibility study pending an isolated auxiliary interface (ISO 6469-3, FMVSS 305). Against the surveyed references [1 - 45], it is the only reported non-isolated three-input three-output converter incorporating DTC-SVM traction control; future work targets soft switching, interleaving of L1, and thermal modeling for continuous automotive duty.

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On behalf of all authors, the corresponding author states that there is no conflict of interest. The authors also confirm that no external funding was received for this work.

References

[1] M. Hemachandran, and R. Madhusudhanan, "Multi Port Single Stage Power Electronics Converter and Wind PFC Converter for DC Micro Grid Applications," *Research Journal of Applied Sciences, Engineering and Technology*, vol. 8, no. 7, pp. 829-836, 2014. [CrossRef] [Google Scholar] [Publisher Link]

[2] T.K. Santhosh, and C. Govindaraju, "Simulation and Analysis of a Four Port DC/DC Converter for Hybrid Electric Vehicle," *2014 Power and Energy Systems: Towards Sustainable Energy*, Bangalore, India, pp. 1-5, 2014. [CrossRef] [Google Scholar] [Publisher Link]

[3] Laura Albiol-Tendillo et al., "Seamless Sliding-Mode Control for Bidirectional Boost Converter with Output Filter for Electric Vehicles Applications," *IET Power Electronics*, vol. 8, no. 9, pp. 1808-1816, 2015. [CrossRef] [Google Scholar] [Publisher Link]

[4] T.K. Santhosh, K. Natarajan, and C. Govindaraju, "Synthesis and Implementation of a Multi-Port DC/DC Converter for Hybrid Electric Vehicles," *Journal of Power Electronics*, vol. 15, no. 5, pp. 1178-1189, 2015. [CrossRef] [Google Scholar] [Publisher Link]

[5] Furkan Akar et al., "A Bidirectional Nonisolated Multi-Input DC-DC Converter for Hybrid Energy Storage Systems in Electric Vehicles," *IEEE Transactions on Vehicular Technology*, vol. 65, no. 10, pp. 7944-7955, 2016. [CrossRef] [Google Scholar] [Publisher Link]

[6] C. Balaji et al., "A Four Port Non-Isolated Multi Input Single Output DC-DC Converter Fed Induction Motor," *2017 IEEE 6th International Conference on Renewable Energy Research and Applications*, San Diego, CA, USA, pp. 631-637, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[7] Kenichi Itoh, Shuntaro Inoue, and Masanori Ishigaki, "28 W/cm³ High Power Density Three-Port DC/DC Converter Cell for Dual-Voltage 12-V/48-V HEV Subsystem," *IEICE Electronics Express*, vol. 14, no. 19, pp. 1-7, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[8] Wilmar Martinez et al., "Total Volume Evaluation of High-Power Density Non-Isolated DC-DC Converters with Integrated Magnetics for Electric Vehicles," *IET Power Electronics*, vol. 10, no. 14, pp. 2010-2020, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[9] A. Geetha et al., "Design of PI Controlled Non Isolated Bidirectional DC to DC Converter for Electric Vehicle Application," *Journal of Physics: Conference Series*, vol. 1000, no. 1, pp. 1-6, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[10] Bang Le-Huy Nguyen et al., "Family of Integrated Multi-Input Multi-Output DC-DC Power Converters," *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata, Japan, pp. 3134-3139, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[11] Padmanaban Sanjeevikumar et al., *Non-Isolated Sextuple Output Hybrid Triad Converter Configurations for High Step-up Renewable Energy Applications*, Advances in Power Systems and Energy Management, Springer, vol. 436, pp. 1-12, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[12] Duong Tran et al., "Optimized Multiport DC/DC Converter for Vehicle Drivetrains: Topology and Design Optimization," *Applied Sciences*, vol. 8, no. 8, pp. 1-17, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[13] Veera Venkata Subrahmanya Kumar Bhajana, Pavel Drabek, and Rajesh Thumma, "Analysis and Design of a High Gain Non-Isolated Zero Current Switching Bidirectional DC-DC Converter for Electric Vehicles," *Automation: Journal of Automation, Measurement, Electronics, Computing and Communications*, vol. 60, no. 1, pp. 79-90, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[14] Sajib Chakraborty et al., "DC-DC Converter Topologies for Electric Vehicles, Plug-in Hybrid Electric Vehicles and Fast Charging Stations: State of the Art and Future Trends," *Energies*, vol. 12, no. 8, pp. 1-43, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[15] Balaji Chandrasekar, Chellammal Nallaperumal, and Subranshu Sekhar Dash, "A Nonisolated Three-Port DC-DC Converter with Continuous Input and Output Currents based on Cuk Topology for PV/Fuel Cell Applications," *Electronics*, vol. 8, no. 2, pp. 1-18, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[16] Kazem Varesi et al., "Design and Analysis of a Developed Multiport High Step-up DC-DC Converter with Reduced Device Count and Normalized Peak Inverse Voltage on the Switches/Diodes," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5464-5475, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[17] Mohammad Raja Al-Soeidat et al., "A Reconfigurable Three-Port DC-DC Converter for Integrated PV-Battery System," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, pp. 3352-3357, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[18] Mohammad Al-Soeidat et al., "A Novel High Step-up Three-Port Bidirectional DC/DC Converter for PV-Battery Integrated System," *IEEE Applied Power Electronics Conference and Exposition*, New Orleans, LA, USA, pp. 3352-3357, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[19] R. Amaleswari, and M. Prabhakar, "Non-Isolated Multi-Input DC-DC Converter with Current Sharing Mechanism," *International Journal of Electronics*, vol. 108, no. 2, pp. 237-263, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[20] Ratil H. Ashique, "A Review of High Efficiency Non-Isolated DC-DC Power Converters for Electric Vehicle Charging Application," *GUB Journal of Science and Engineering*, vol. 6, no. 1, pp. 60-74, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[21] Saikumar Bairabathina, and S. Balamurugan, "Review on Non-Isolated Multi-Input Step-up Converters for Grid-Independent Hybrid Electric Vehicles," *International Journal of Hydrogen Energy*, vol. 45, no. 41, pp. 21687-21713, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[22] Balaji Chandrasekar et al., "Non-Isolated High-Gain Triple Port DC-DC Buck-Boost Converter with Positive Output Voltage for Photovoltaic Applications," *IEEE Access*, vol. 8, pp. 113649-113666, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[23] Triptendu Chaudhury, and Debaprasad Kastha, "A High Gain Multiport DC–DC Converter for Integrating Energy Storage Devices to DC Microgrid," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10501-10514, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[24] Mena ElMenshawy, and Ahmed Massoud, "Hybrid Multimodule DC-DC Converters for Ultrafast Electric Vehicle Chargers," *Energies*, vol. 13, no. 18, pp. 1-28, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[25] Mena ElMenshawy, and Ahmed Massoud, "Modular Isolated DC-DC Converters for Ultra-Fast EV Chargers: A Generalized Modeling and Control Approach," *Energies*, vol. 13, no. 10, pp. 1-34, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[26] Tohid Jalilzadeh et al., "Multiport DC-DC Converter with Step-up Capability and Reduced Voltage Stress on Switches/Diodes," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11902-11915, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[27] Tohid Jalilzadeh et al., "Bidirectional Multi-Port DC-DC Converter with Low Voltage Stress on Switches and Diodes," *IET Power Electronics*, vol. 13, no. 8, pp. 1593-1604, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[28] Vafa Marzang et al., "A High Step-up Nonisolated DC-DC Converter with Flexible Voltage Gain," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10489-10500, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[29] Josep M. Olm et al., "Adaptive Control-based Voltage Regulation of a Magnetically Coupled Multiport DC-DC Converter for Electrified Vehicles Applications," *2020 IEEE International Symposium on Circuits and Systems*, Seville, Spain, pp. 1-5, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[30] Prajof Prabhakaran, and Vivek Agarwal, "Novel Four-Port DC-DC Converter for Interfacing Solar PV-Fuel Cell Hybrid Sources with Low-Voltage Bipolar DC Microgrids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1330-1340, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[31] Sridhar Ramasamy, Ilambirai Raghavan Chandran, Chellammal Nallaperumal, "A High Voltage Gain Multiport Zeta-Zeta Converter for Renewable Energy Systems," *Informacije MIDEM-Journal of Microelectronics, Electronic Components and Materials*, vol. 50, no. 3, pp. 215-230, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[32] Sajad Rostami et al., "Three-Port DC-DC Converter based on Quadratic Boost Converter for Stand-Alone PV/Battery Systems," *IET Power Electronics*, vol. 13, no. 10, pp. 2106-2118, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[33] Yusuke Sato, Masatoshi Uno, and Hikaru Nagata, "Nonisolated Multiport Converters based on Integration of PWM Converter and Phase-Shift-Switched Capacitor Converter," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 455-470, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[34] Murat Mustafa Savrun, and Alihan Atay, "Multiport Bidirectional DC-DC Converter for PV Powered Electric Vehicle Equipped with Battery and Supercapacitor," *IET Power Electronics*, vol. 13, no. 17, pp. 3931-3939, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[35] R.B. Selvakumar, C. Vivekanandan, and S. Kavitha, "Two-Quadrant Current Reversible Non-Isolated DC-DC Converter for Plug-in Electric Vehicle Chargers," *AIP Conference Proceedings*, vol. 2207, no. 1, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[36] Arulmozhi Subramanian, and K.R. Santha, "Review of Multiport Isolated Bidirectional Converter Interfacing Renewable and Energy Storage Systems," *International Journal of Power Electronics and Drive Systems*, vol. 11, no. 1, pp. 466-476, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[37] Dai-Duong Tran et al., "NSGA-II-based Codesign Optimization for Power Conversion and Controller Stages of Interleaved Boost Converters in Electric Vehicle Drivetrains," *Energies*, vol. 13, no. 19, pp. 1-31, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[38] Shreyansh Upadhyaya et al., "Modelling and Control of Non-Isolated Multiport DC/DC Converter," *2020 First IEEE International Conference on Measurement, Instrumentation, Control and Automation*, Kurukshetra, India, pp. 1-5, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[39] Yu-En Wu, and Xiu-Yi Lin, "A Novel Non-Isolated Three-Port Bidirectional DC/DC Converter for Photovoltaic Electric Scooter Charging Stations," *Electronics*, vol. 9, no. 10, pp. 1-23, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[40] Neda Zahedi Saadabad et al., "New Soft-Switched High Gain Three-Port DC–DC Converter with Coupled Inductors," *IET Power Electronics*, vol. 13, no. 19, pp. 4562-4571, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[41] Yun Zhang et al., "A Switched-Capacitor Interleaved Bidirectional Converter with Wide Voltage-Gain Range for Super Capacitors in EVs," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1536-1547, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[42] Abdulaziz Almutairi et al., "Multi-Port PWM DC-DC Power Converter for Renewable Energy Applications," *Energies*, vol. 14, no. 12, pp. 1-22, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[43] Elham Amiri et al., "Multi-Input High Step-up DC–DC Converter with Independent Control of Voltage and Power for Hybrid Renewable Energy Systems," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 12, pp. 12079-12087, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[44] Iman Askarian, Majid Pahlevani, and Andrew M. Knight, "Three-Port Bidirectional DC/DC Converter for DC Nanogrids," *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 8000-8011, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[45] Ishita Biswas, Debaprasad Kastha, and Prabodh Bajpai, "Small Signal Modeling and Decoupled Controller Design for a Triple Active Bridge Multiport DC-DC Converter," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1856-1869, 2021. [CrossRef] [Google Scholar] [Publisher Link]

[46] Giuseppe S. Buja, and Marian P. Kazmierkowski, "Direct Torque Control of PWM Inverter-Fed AC Motors-A Survey," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 4, pp. 744-757, 2004. [CrossRef] [Google Scholar] [Publisher Link]

[47] Cristian Lascu, Ion Boldea, and Frede Blaabjerg, "A Modified Direct Torque Control for Induction Motor Sensorless Drive," *IEEE Transactions on Industry Applications*, vol. 36, no. 1, pp. 122-130, 2000. [CrossRef] [Google Scholar] [Publisher Link]