VLSI Implementation of CDMA systemUsing Vedic Multiplier based on Urdhva–Tiryakbhyam Sutra

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Abstract

This paper anticipated the design of a novel Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics that have been modified to improve performance of CDMA communication system . Code-division multiple access (CDMA) is a channel access method used by various radio communication technologies. CDMA is an example of multiple access, where several transmitters can send information simultaneously over a single communication channel. A high speed CDMA system depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing system as well as in general processors. Currently the speed of the multipliers is limited by the speed of the adders used for partial product addition. In this paper, we proposed an 8-bit multiplier using the new methodology of Vedic Mathematics called as Urdhva-Tiryagbhyam sutra which is used for generating the partial products. The partial product addition in Vedic multiplier is realized using carry-skip technique. This paper depicts the design of an efficient 8×8 binary arithmetic multiplier by using Vedic Mathematics. From various multiplication techniques, Urdhva-Tiryagbhyam sutra is being implemented because this sutra is applicable to all cases of algorithms for N×N bit numbers and the minimum delay is obtained. A 4×4 Vedic Multiplier is designed using 9 –full adder and a special 4-bit adder which is having reduced delay. Then 8-bit multiplier is designed using four 4-bit multiplier and 3-ripple carry adder. Then 8×8 Vedic Multiplier is coded in VHDL, synthesized and simulated using Xilinx ISE8.2 Software. Finally the objective of this paper lies in design of an efficient vedic multiplier using Urdhva–Tiryakbhyam Sutra in VHDL Environment.

I. INTRODUCTION

Code Division Multiple Access (CDMA) is a sort of multiplexing that facilitates various signals to occupy a single transmission channel. It optimizes the use of available bandwidth. The technology is commonly used in ultra-high-frequency (UHF) cellular telephone systems, bands ranging between the 800-MHz and 1.9-GHz.Code Division Multiple Access system is very different from time and frequency multiplexing. In this system, a user has access to the whole bandwidth for the entire duration. The basic principle is that different CDMA codes are used to distinguish among the different users. Techniques generally used are direct sequence spread spectrum modulation (DS CDMA), frequency hopping or mixed CDMA detection (JDCDMA). Here, a signal is generated which extends over a wide bandwidth. A code called spreading code is used to perform this action. Using a group of codes, which are orthogonal to each other, it is possible to select a signal with a given code in the presence of many other signals with different orthogonal codes.

CDMA allows up to 61 concurrent users in a 1.2288 MHz channel by processing each voice packet with two PN codes. There are 64 Walsh codes available to differentiate between calls and theoretical limits. Operational limits and quality issues will reduce the maximum number of calls somewhat lower than this value. In fact, many different "signals" baseband with different spreading codes can be modulated on the same carrier to allow many different users to be supported. Using different orthogonal codes, interference between the signals is minimal. Conversely, when signals are received from several mobile stations, the base station is capable of isolating each as they have different orthogonal spreading code.

A multiplier is one of the key hardware blocks in most digital signal processing (DSP) systems. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications and spectral analysis (Ayman.A et al (2001)). Many current DSP applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints. Since multipliers are rather complex circuits and must typically operate at a high system clock rate, reducing the delay of a multiplier is an essential part of satisfying the overall design.

Multiplications are very expensive and slows the over all operation. The performance of many computational problems are often dominated by the speed at which a

multiplication operation can be executed. Consider two unsigned binary numbers X and Y that are M and N bits wide, respectively

Related work

Ren Der Chen briefelydescribe two designs of low-error fixed-width signmagnitudeparallel multipliers and two's-complement parallel multipliersfor digital signal processing applications are presented Swartzlander, Jr.presented a technique for parallel multiplication which computes the product of twonumbers by summing only the most significant columns of the multiplicationmatrix, along with a correction constant

II. EXISTING SCHEME

we target the design of power–error efficient multiplication circuits. We differ from the previous works by exploring approximation on the generation of the partial products. The proposed method can be easily applied in any multiplier architecture without the need for a special design, in contrast to related works. In addition, the error imposed by perforation depends only on the configuration parameters and, in contrast to existing work, can be analytically calculated without the need for exhaustive simulations.

$$A \times B = \sum_{i=0}^{n-1} Ab_i 2^i, \;\; b_i \in \{0, 1\}.$$

$$A \times B|_{j,k} = \sum_{\substack{i=0, \\ i \notin [j, j+k)}}^{n-1} Ab_i 2^i, \;\; b_i \in \{0, 1\}.$$

the partial product perforation method for the design of approximate hardware multipliers is described. Consider two n-bit numbers A and B. The result of their multiplication A × B is obtained after summing all the partial products Abi, where bi is the ith bit of B. Thus The partial product perforation technique omits the generation of k successive partial products starting from the j th one. A perforated partial product is not inserted in the accumulation tree, and hence n full adders can be eliminated. Applying the product perforation with j and k configuration values on the multiplication, A × B produces the approximate result For each architecture, the dot diagrams of the accurate and the respective perforated tree are presented. The dots represent the bits of the partial products that have to be accumulated, while the stages represent the delay of the reduction process followed by each tree. The dashed boxes with four dots are 4:2 compressors, those with three are full adders and those with two are either full- or half-adders. Through the proposed approximation technique, the power, area, and delay of the multiplication circuit are decreased, making, though, the computation imprecise. The higher the order of a perforated partial product, the greater the error imposed at the final result

III. PROPOSED SYSTEM

This paper anticipated the design of a novel Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics that have been modified to improve performance. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing system as well as in general processors. Currently the speed of the multipliers is limited by the speed of the adders used for partial product addition. In this paper, we proposed an 8-bit multiplier using the new methodology of Vedic Mathematics called as Urdhva-Tiryagbhyam sutra which is used for generating the partial products. The partial product addition in Vedic multiplier is realized using carry-skip technique. This paper depicts the design of an efficient 8×8 binary arithmetic multiplier by using Vedic Mathematics. From various multiplication techniques, Urdhva-Tiryagbhyam sutra is being implemented because this sutra is applicable to all cases of algorithms for N×N bit numbers and the minimum delay is obtained. A 4×4 Vedic Multiplier is designed using 9 –full adder and a special 4-bit adder which is having reduced delay.

Vedic mathematics is the name given to the ancient system of mathematics which was rediscovered from the Vedas. In compare to conventional mathematics Vedic mathematics is simpler and easy to understand. Swami Bharati Krishna TirthajiMaharaj (1884-1960), re-introduced the concept of ancient system of Vedic mathematics .

The word 'Vedic' is resultant from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics includes sixteen-sutras or formulae and thirteen sub-sutras. Various applications of Vedic mathematics includes theory of numbers, compound multiplication, algebraic operation, calculus, squaring, cubing, cube root, simple quadratic, coordinate geometry and wonderful Vedic Numeric Code .

Vedic mathematics is a domain which presents various effective algorithms that can be applied in different branches of engineering such as digital signal processing and computing. Most common multiplication algorithms in math coprocessor are array and booth multiplication algorithm. Due to the parallel calculation of the partial products the array multiplier takes less computation time. For high speed multiplication large booth arrays having partial sum and carry register is required.

4-Bit Multipliers The 4×4 Vedic multiplier in binary is implemented by using VERILOG code.In order to reduce the delay of 4×4 multiplier, it is designed by using nine full adders and a 4-bit special adder.

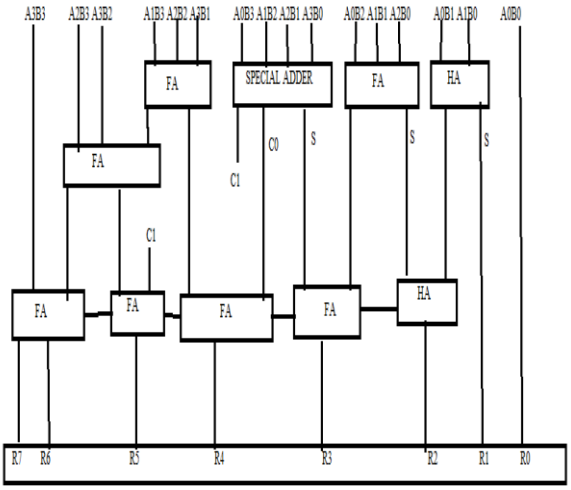


Fig: Architecture of 4×4 Vedic Multiplier Special Adder in 4*4 multiplier

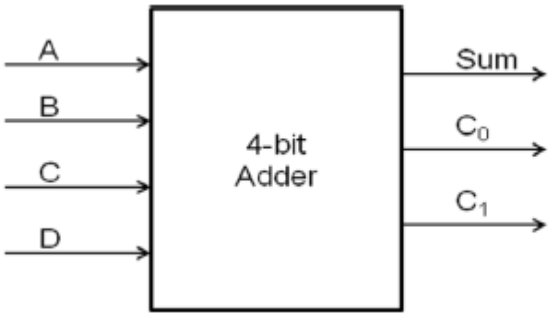


Fig: Architecture of 4-Bit special adder.

In the figure A,B,C,D are four inputs.C0 and C1 are LSB and MSB of carry outputs respectively and Sum is the sum of four inputs. The Boolean expressions for the same are given below. Sum<= p XOR q XOR r XOR s c0<= ((NOT q) AND s)OR (r AND (NOT s))OR (q AND (NOT r)) c1<= p AND q AND r AND s

UrdhvaTiryakbhyam method

It is another method used for multiplication of complex number. UrdhvaTiryakbhyam method means ―vertically and crosswise‖. Vertically means straight above multiplication and crosswise means diagonal multiplication and taking their sum. It has advantage that it reduces the multi bit multiplication into single bit multiplication and addition. This results in generation of all the partial products in one step which further reduces carry propagation that occurs from LSB to MSB during the process of addition. We can either implement this sutra starting from right hand side or from left hand side.

The straight above multiplication and diagonal multiplication and taking their addition in UrdhvaTiryakbhyam method in case of two four bit numbers a and b can be better understand from step 1 to step 7 as shown in figure below.

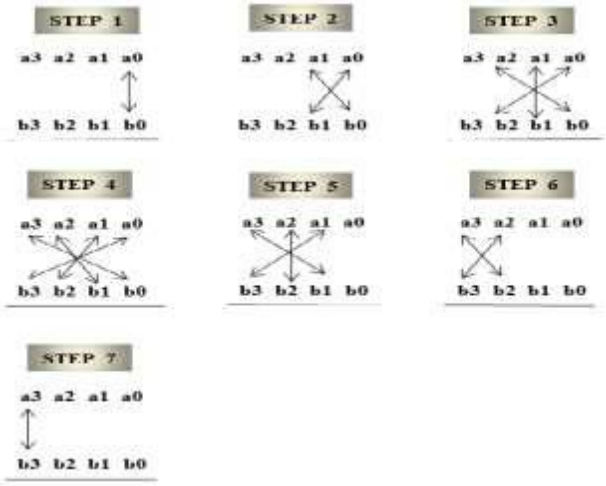


Fig : Line diagram of UrdhvaTiryakbhyam Sutra (method) for 4 x 4 binary number multiplication.

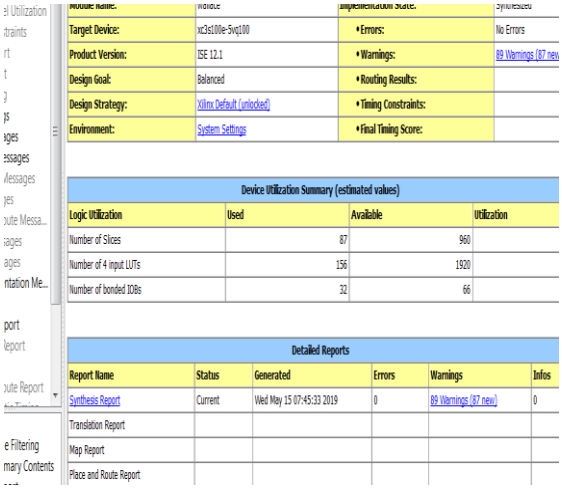
Let us take an example of two four bit binary numbers a and b by applying vertically and crosswise method to it, as shown in figure.

p0 = a0b0 ---------- (I)
s1p1 = a1b0 + a0b1 ---------- (II)
s2p2 = s1 + a2b0 + a1b1 + a0b2 ---------- (III)
s3p3 = s2 + a3b0 + a2b1 + a1b2 + a0b3 ---------- (IV)
s4p4 = s3 + a3b1 + a2b2 + a1b3 ---------- (V)
s5p5 = s4 + a3b2 + a2b3 ---------- (VI)
s6p6 = s5 + a3b3 ---------- (VII)

From equation no. (I) to (VII), the final result can be obtained as s6p6p5p4p3p2p1p0.

IV. IMPLEMENTATION RESULTS

A. Existing system:



Target Device:	xc3s100e-5vq100	• Errors:	No Errors
Product Version:	ISE 12.1	• Warnings:	89 Warnings (87 new
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

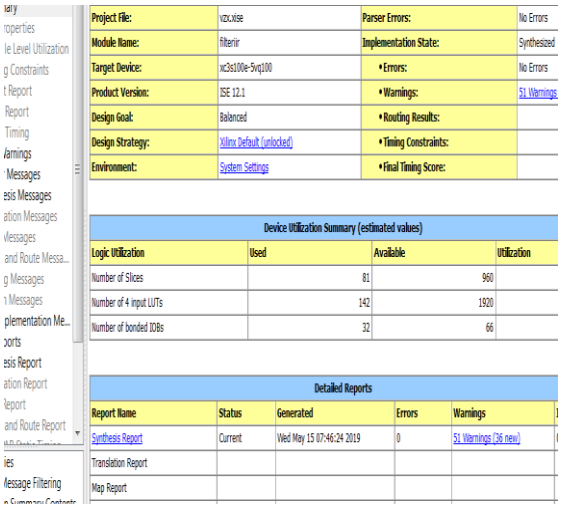
Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slices	87	960	
Number of 4 input LUTs	156	1920	
Number of bonded IOBs	32	66	

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Wed May 15 07:45:33 2019	0	89 Warnings (87 new)	0
Translation Report					
Map Report					
Place and Route Report					

B. Proposed System:



Project File:	vzx.xise	Parser Errors:	No Errors
Module Name:	filteriir	Implementation State:	Synthesized
Target Device:	xc3s100e-5vq100	• Errors:	No Errors
Product Version:	ISE 12.1	• Warnings:	51 Warnings
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slices	81	960	
Number of 4 input LUTs	142	1920	
Number of bonded IOBs	32	66	

Detailed Reports

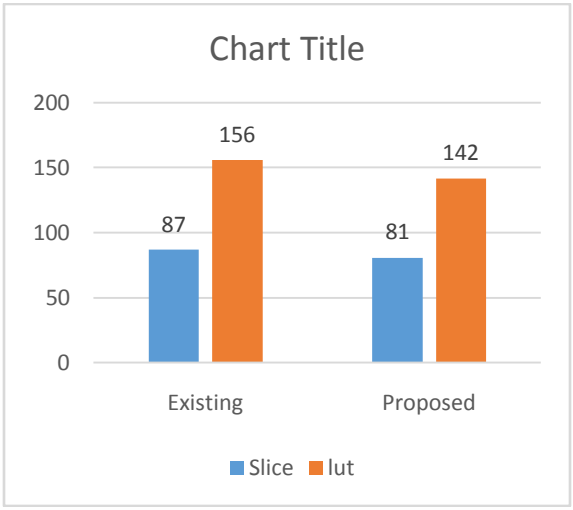
Report Name	Status	Generated	Errors	Warnings
Synthesis Report	Current	Wed May 15 07:46:24 2019	0	51 Warnings (36 new)
Translation Report				
Map Report				

The proposed has been simulated and the synthesis report can be obtained by using Xilinx ISE 12.1i. The various parameters used for computing existing and proposed systems with Spartan-3 processor are given in the table 7.1.

s.no	Parameter	Existing	Proposed
1	Slice	87	81
2	lut	156	142

V. PERFORMANCE ANALYSIS

The Figure given below is shown that there is a considerable reduction in time and area based on the implementation results which have been done by using Spartan-3 processor. The proposed algorithm significantly reduces area consumption when compared to the existing system.



VI. CONCLUSION

Multiplier is basic key component of CDMA system . The proposed Vedic Multiplier circuit using Urdhva-Tiryakbhyam Sutra can be implemented in arithmetic and logical units of a DSP processor replacing the traditional circuits. Generally the Vedic multipliers are much faster than the conventional multipliers. This gives us scheme for hierarchical multiplier design. So the design density gets condensed for inputs of large no of bits and modularity gets augmented .In summary, embodiments of the investigation provided in this work have led to the design of vedic multiplier for binary numbers using Urdhva-TiryakbhyamSutra.Urdhvatiryakbhyam, Nikhilam and Anurupye sutras are such vedic Sutras which can reduce the delay, power and hardware requirements for multiplication of numbers.Hence the designed multiplier can be used in various applications like digital signal processing,VLSI Signal Processing,encryption and decryption algorithms in cryptography etc.The proposed design can further be implemented for16x16,32x32 multipliers and their performance comparision with the help of FPGA.

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