Carry Skip Adder Using Carry Save Adder Logic

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Abstract-In the digital design circuits the adders plays a vital role not only for addition it also used in filter designing, multiplexing and division. sThis paper gives the comparison of parallel adder and proposed a hybrid adder circuit. By using this hybrid adder circuit to improve the speed. To diminish the propagation delay here Carry Save Adder (CSA) and Carry Skip Adder (CSKA) are used. The result shows the reduction in the propagation delay.

Key--words *-Ripple Carry Adder (RCA), Carry Save Adder (CSA), Carry Skip Adder (CSKA), Propagation Delay, Hybrid Adder*.

I. INTRODUCTION

Now-a-days, it is essential to diminish the expenditure of the power and size of the device, to increase the device operation speed. The demand of the low power VLSI has been increased in mobile communication. So that the design of the device, consider the less silicon area, high speed and low power expenditure. Mathematically, the Arithmetic Logic Unit (ALU) and Floating Point Unit (FPU) plays an essential role. ALU performs the Arithmetic operation such as Add, Sub, Mul, Div and Logical Operations like AND, OR and INV and Command comparison.

Firstly, we are using Half Adder it contains 2- inputs and 2-outputs namely sum and carry. Next using of simple Full Adder with 2- inputs and cin then it gives 2-outputs sum and carry, but it is for single bit. For multi bit we are using full adder are connected in parallel and the sum of each bit done consecutively and the carry bit has given as a input to the next block. Then the outcome of the final carry is calculated.

Here various adders are used namely Ripple Carry Adder(RCA), Carry Look Ahead Adder (CLA), Carry Increment Adder (CIA), Carry Skip Adder (CSKA), Carry Save Adder (CSA) etc. RCA is the simple adder that contains the FA which are connected in the equivalent form.

CLA is known as fast adder are mainly used in digital circuits. CLA define the carry bits by increasing the speed and reduces the amount of time. In CSA, each stage carry bits are saved. Thus, the delay in CSA is constant because carry is not propagated. At the output the CAS all the saved carry bits needed to be added to all the sum's to obtain an N-bit sum.

A carry-skip adder well-known as carry-bypass adder. The implementation of this sadder improves the delay of a ripple-carry adder. The improvement of the worst-case delay is succeeded by using a number of carry-skip adders to obtain a block-carry-skip adder. When compared all adders CIA is best regarding the problems. CIA contain set of two RCA blocks of 4-bits and having increment block of HA.

By using Hybrid Adders, which contains more expenditure of the power and reduced delay when compared to further adders. CIA-RCA, CIA-CLA are the Hybrid Adders are available. But, here we using the CSA and CSKA acts as proposed Hybrid Adder to improve the propagation delay.

The outstanding unit of the paper is shown as follows: Unit II gives complete literature analysis of the preceding work. In unit III we discussed about the basic concepts of RCA, CSA, CSKA Adder. In unit IV we discussed about the proposed Hybrid Adder. In unit V discussed about the helpfulness of the proposed adder with new result. Finally, the conclusion of the paper is discussed in the unit VI.

II. LITERATURE REVIEW

So many methods have been done so far interrelated to these problems of the adder [1] [3] [5]. Basic theory of adder is deliberated in [4, 6, 8]. Paper [11] defined 32-bit FA. It is multiplexer based adder. Arithmetic Logic Unit(ALU) and Floating Point Unit (FPU)are with

esteem to adder design is defined in [2]. The manipulative of the ALU is responsible for the speed up the circuit.

Carry Skip Adder [10] is a higher bit adder operation in which carry can be skip to the following block. It gives the circuit result, as decrease in the gate delay and there is no delay in propagation. In this paper using 2-bit Skip block, 4-bit Skip block or 8-bit Skip Logic for manipulative the 16-bit CSKA. The 4-bit skip block most active with respect to the delay and power consumption.

In CSA [1 ,3 ,5] it contains the two full adders with respect to RCA. CSA have the main benefit that can operate with three inputs. In the first stage it save the carry and send it to the next stage. Next we are consider the proposed system that is Hybrid Adder that contain two adders related to each other and perform similar as the CLA-RCA and CIA-CLA.

III. FUNDAMENTALS OF RCA, CSA AND CSKA ADDER

A. Ripple Carry Adder (RCA)

A RCA is a logic circuit in which the Cout of each FA is given as a Cin to the next successive FA so that it is known as ripple carry adder. Block diagram of a 4-bit RCA is shown below fig. 1.

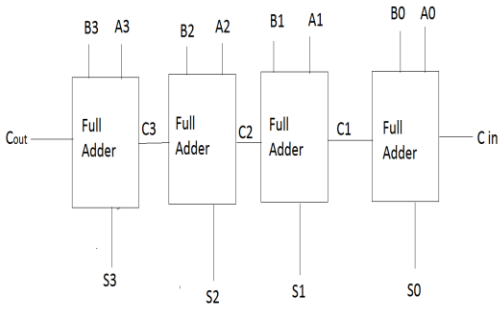

Fig. 1. 4-bit RCA

Now consider an two 4-bit inputs: A= 1 0 1 0; and B= 1 0 1 1 for addition operation. Here A0=0 and B0=1, so first addition will follow in the first full adder (FA) block and get S0=1 and C1=0. Now this C1 will disseminate to the succeeding block as Cin. For 2nd FA block inputs areas A1=1 and B1=1 and C1=0, so the S1=0 and carry C2=1which will disseminate to the 3rd block. By this process we getS2=1, and C2=0 and S3=0 and C3=1. So finally we get carry-out=1 as an output.

	1	0	1	0
+1	0	1	1	
1	0	1	0	1

B

- ***Carry Save Adder (CSA):***

Carry Save Adder is also called as parallel RCA adder. In CSA, the carry bits are saved at each stage. Thus, the delay of a CSA is constant because there is no carry propagation is present. At the final stage all the carry bits should be added to obtained N-bit sum. consider an example of 4bit CSA having inputs: A=1 0 0 1; and B=1 1 1 0. The graphic diagram of CSA as shown in below fig.2.

A=	1	0	0	1
B=	1	1	1	0
IC=	1	0	0	0
IS=		0	1	1	1
SUM=	1	0	1	1	1

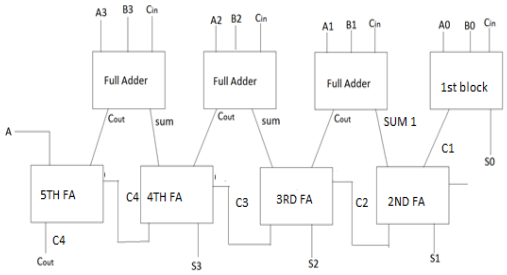

Fig. 2. 4-bit CSA

Advantages of CSA:

• we can perform 3 different numbers at a time in CSA.

• The carry is not propagated in CSA instead of propagation it stores the carry bit in current stage and performs the addition at the final stage.

Disadvantages:

•CSA performes better in higher bits rather than lower bits operation because at lower bit it gives high propagation delay, power consumption.

• increased area because of the large Transistor count.

C. Carry Skip Adder (CSKA):

It is the fastest adder when compared to RCA. It contains RCA which is used to increase the speed of the carry chain. A carry-skip adder also known as a carry-bypass adder the implementation of this adder reduce the delay of a RCA . The improvement of the worst-case delay is succeeded by using number of carry-skip adders to obtain a block-carry-skip adder.

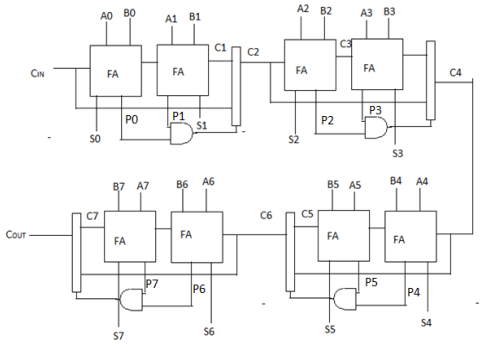

Fig. 3. 8-bit CSKA

Here Carry Skip Adder can be distributed into many blocks for 16-bit operation. The below fig3, fig4 and fig5 shows the 8bit adder, 16bit adder, 32bit adder.

2 block CSKA:

For 16-bit operation we use two RCA block. Here the first RCA perform the basic summation and next block perform the summation and have a Carry Skip chain.

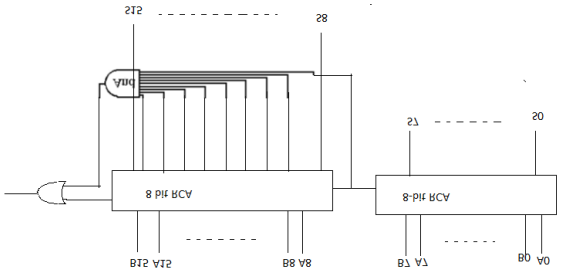

Fig. 4. 4-bit CSKA with 2 block

4 block CSKA:

According to the 2 block CSKA we can design 4 block CSKA and 8 block CSKA by using 4 bit RCA and 2 bit RCA block respectively. When compared to all adders 8 block adder having less delay and 2 block adder having less power consumption. But in this paper we are study about the delay so that we consider the 8 block CSKA. The design of 8 blocks CSKA is shown below.

The carry skip adder has a skip logic block that can increase the speed of the adder. There are two types of carry skip logic as shown in below fig.6 and fig.7.

Skip Logic Circuit:

Consider the 2-bit operation for a skip logic circuit as shown in below fig6. This can be replaced by OR gate.

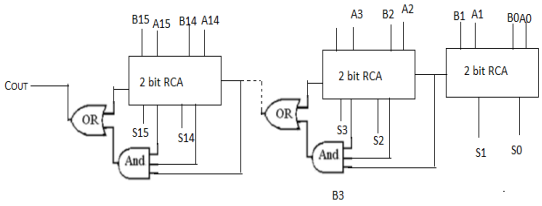

Fig. 5. 2 bit RCA block in 8 block CSKA

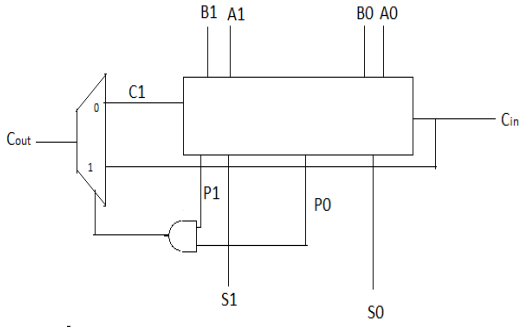

Fig. 6. Skip Logic in 2-bit CSKA

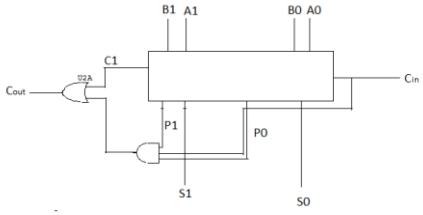

Fig. 7. Skip Logic using OR gate

Advantages:

- In higher bit operation the circuit response is good.
- When compare to other circuits skip logic circuit is faster.
- FA circuit produces the pi logic circuit.

Disadvantages:

• We require 2 carry skip logic circuit for 4-bit operation which makes the adder more.
• It has high delay, power consumption in lower bit operation.

IV. PROPOSED HYBRID ADDER

Hybrid 4-bit adder is shown in fig.8.

Working process:

Consider the FA circuit that having the 2-inputs and a carry and produces the sum and Cout. But in the case of CSA we are using 2-inputs and one carry –in port as the another input operand so that we can perform the operation on the numbers that produces the 2-outputs sum and carry that acts as the 2-inputs A and B. To implement the two input operation, consider, HA which is used to reduce the propagation delay and that HA produces the sum and carry passes through the CSKA circuit with skip logic.

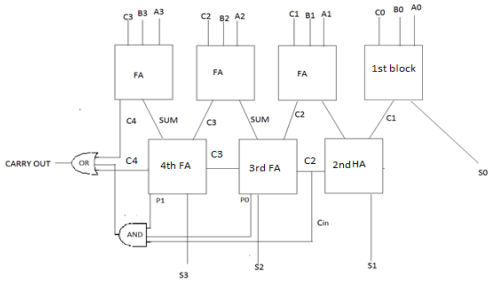

Fig. 8. 4- bit proposed circuit

Advantages of the proposed circuit:

• The advantage of proposed circuit is mixture of two adders like Carry Save Adder it can perform the three inputs operation and Carry Skip Adder is used to skip the carry in order to speed up the calculation.
• After the first stage in CSA we can use the simple RCA for calculation, but instead of RCA we can use CSKA for more efficient operation.
• For 4-bit operation we require 2 carry skip logic circuit in CSKA that causes the more complexity. But in the case of proposed circuit we require one skip block that reduces the circuit complexity.
• In order to develop the pi block we require a XOR block, but in the case of proposed circuit we use the XOR circuit that are obtained from the adder block which reduces the delay and number of gates.

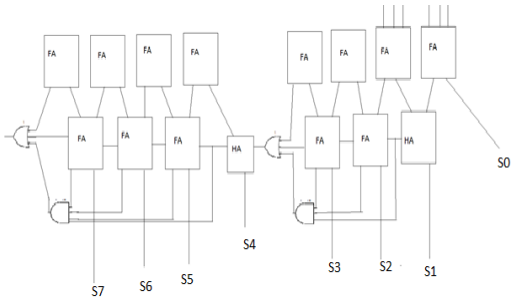

Fig. 9. 8-bit proposed circuit

Delay Calculation:

Let us assume XOR has 2 gate delay and AND, OR has 1 gate delay each. Consider the FA circuit as shown in figure.10. It has two XOR gate delay (4 gate delay) from A, B to SUM and one XOR gate delay (2 gate delay) from Cin to SUM. Similarly, it has 1 XOR, 1 AND, 1OR delay (4 gate delay) from Cin to carry out.

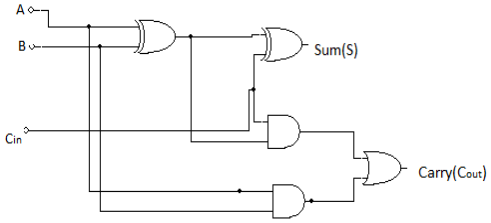

Fig. 10. Full Adder diagram

Next, consider the HA shown in figure.11. In a half adder, it has 1 XOR delay (2 gate delay) from A, B to SUM and we have 1 gate delay from A, B to carry.

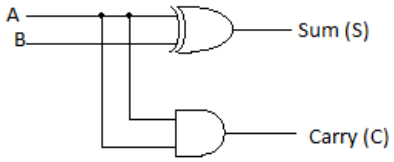

Fig. 11. Half Adder diagram

Next, consider the CSA circuit in fig.2. In first block it has 4 gate delay from A0, B0, C0 to C1 and in the 2nd FA block it has 4 gate delay from C1 to C2 and this C1 act as an operand and 2 gate delay from C2 to C3 like this we have 2 gate delay each from 3rd FA and 5th FA. Finally, in the 5th FA block we have 2 gate delay from C4 to C5. Then the total delay=4+4+2+2+2=14 gate delay for 4bit CSA.

Now, consider the proposed circuit shown in fig.8. We know that in the 1st block it has 4 gate delay from A0, B0, C0 to C1. But coming to the 2nd HA block C1 acts as an operand and it has 1 gate delay to produce C2. Here C2 goes through the skip logic circuit and it has 2 gate delay (1 AND gate delay, 1 OR gate delay). Then

the total delay=4+1+2=7 gate delay for 4bit circuit. Here the gate delay calculation for higher order bits can be obtained by cascading the circuit for multiple times as shown in fig.11.

V. RESULT AND COMPARISON WITH PROPOSED ADDER

TABLE I. Circuit Complexity On The Basis Of Gate Count

Bit	No. of basic gate required			
	RCA	CSA	CSkA	Proposed adder
4-bit	72	72	80	61
8-bit	144	144	160	131
16-bit	288	288	320	271
32-bit	576	576	640	551
64-bit	1152	1152	1280	1111
128-bit	2304	2304	2560	2231

TABLE II. Propagation Delay On The Basis Of Gate Count

No. of bit	Delay on the basis of gate count			
	RCA	CSkA	CSA	Proposed adder
4-bit	20	16	14	8
8-bit	36	28	22	15
16-bit	68	52	38	32
32-bit	132	100	70	52
64-bit	260	196	134	99
128-bit	516	388	262	195

VI. CONCLUSION

In the convention CSKA the delay is reduced parallel to the CSA. While considering the proposed hybrid adder in which CSA is combined with CSKA that reduces the delay when compared to convention circuit.

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