Carry Select Adder using Brent Kung Adder

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Abstract

carry select adder is a precise way to appliance an adder where the carry select adder is the best adder for performing the arithmetic operation because it has the high speed and which requires more area and power.
In the existing system we use the double ripple carry adder and then the we use the binary to excess-1

The Brent kung adder decreases the delay and diminishes area.

Keywords- linear Brunt kung carry select adder, square Root brunt kung carry select adder, modified square root brunt kung carry select adder; less gate counts; 4- bit brunt kung adder; 4-bit binary to excess-1 converters.

I. INTRODUCTION

Adders are the combinational circuits which can perform addition of binary bit. In processors it is used to analyze addresses, table indices, and similar operation. It can be shaped for many numerical illustrations, such as binary coded decimals or excess-3.[1]

We have different adders such as half adders, full adders, ripple adder, carry select adders, carry save adders. In the carry select adder it has ripple carry adders where itcreated with full adders. Full adders consist of two half adders and it is a combinational circuit that has 3 inputs bits to generate a sum bit and a carry bit full adder is usually a component in cascade of adders[1], [2]. where as half adder has two inputs and two outputs.[3]

To compute sum and carry below the category of high speed adders originates in carry select adders. Basic CSLA consists of 2 RCA with different input carry that is carry in = 0 and carry in = 1 and sum ispre-evaluated for both carry in parallel. To select one of the output sum based on output carry of the previous stage using multiplexer. Adders uses multiples pairs of RCA and it occupies more area.

Instead of RCA with carry in = 0 to obtained LBKCSLA the fundamental idea of this task is to use brunt kung adder so it reduces the chip area and over all computation delay.

By having different size groups of BKA and RCA in LBKCSLA. SQRTBKCSLA is obtained.

By replacing RCA with binary to excess-1 converter in SQRTBKCSLA. MSQRTBKCSLA is designed. The lesser number of logic gates of BEC than n-bit full adder yields reduction in chip area and to obtain MSQRTBKCSLA. RCA with carry in = 1 is replaced by BEC.

Part II illustrate the brunt kung adder and part III represents the binary to excess-1 converter logic. In part IV, V, VI the architecture of LBKCSLA, SQRTBKCSLA, MSQRTBKCSLA. Part VII shows the delay and area evaluation. Part VIII shows the simulated results and comparison of CSLA's finally the work is concluded in part IX

II. BRENT KUNG ADDER

The 4-bit BKA is shown fig.1. BKA [5], [6], [7]is parallel adder that consists BKA pre-processing stage. Here BKA parallel prefix adder and BKA post processing stage for calculation of summation and output carry of input bits. BKA [5], [6], [7].

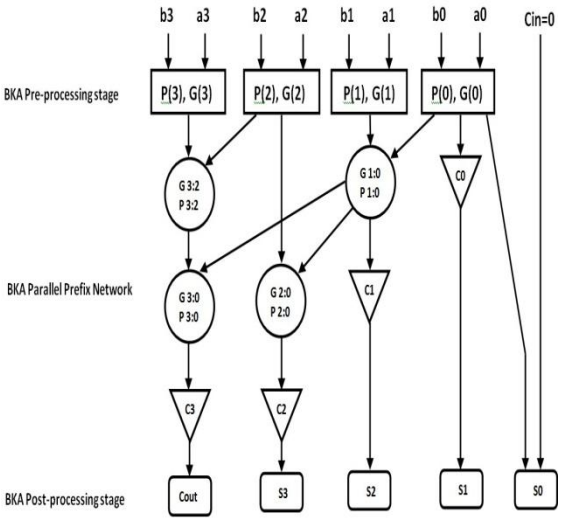

Fig 1: BKA

A. BKA Pre-processing stage

The below figure shows the following equation to compute the signals where the two signals can generate and propagate are computed for the A and B

G(i) = Ai AND Bi; for i = 0, 1, 2,...n-1 where n is the no. of bits
P(i) = Ai XOR Bi; for i = 0, 1, 2,....n-1 where n is the no. of bits

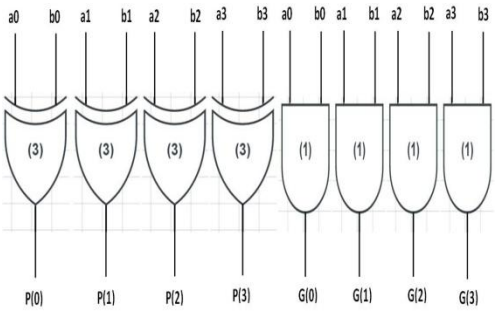

Fig 2: G AND P signals for 4-bit

B. BKA parallel prefix network

The intermediate signals like carry generate and propagate signals are generated for computing carry equivalent to each input as shown in the below figure where the following equations can be given

G1 = G1 OR (P(1)AND G(0));
P1 = P(1) AND P(0);
Gi = G(i) OR (P(i) AND Gi-1); for i = 2, 3...n-1
Pi = P(i) AND Pi-1; for i = 2, 3,....n-1 where n is the no. bits

Carries of each input bit are given by equations:

C0 = G(0);

Ci = Gi; for i = 1, 2,....n-1 where n is no. of input bits

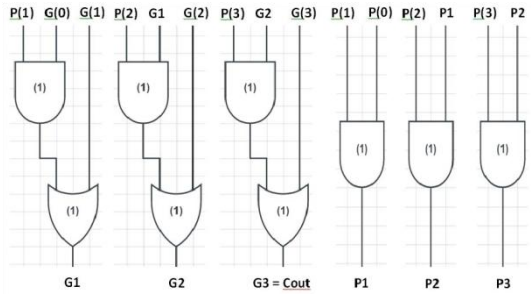

Fig 3 : signals to calculate carries for 4-bit

C. BKA post-processing stage

In this the final sum bits and output carry are computed as shown in the figure and also given some of the equation as follows

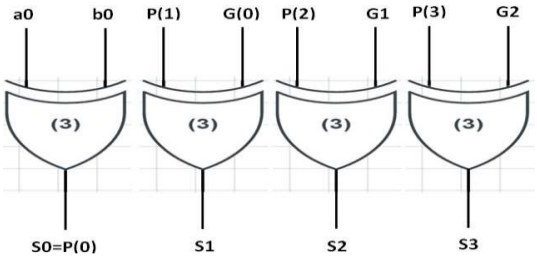

Fig 4 : 4-bit input using BKA

S0 = P(0);

S1 = P(1) XOR G(0);

Si = P(i) XOR Gi-1; for i = 2, 3,..n-1 where n is the no. of bits

Cout = Gn-1; for i = 2,3,...n-1 where n is the no. of bits

III. BINARY TO EXCESS-1 CONVERTER

The carry select adder had been replaced instead of ripple carry adder in order to reduce the logic gates which leads to reduce the chip area as the schematic diagram of 4-bit BEC is shown.BEC[8]

The Boolean expression of 4-bit BEC are shown below

(note: symbols, ~NOT, & AND, ^XOR)

Sum4 = ~S4;

Sum5 = S4^S5;

Sum6 = S6^(S4 & S6);

Carry6 = C6^(S4 & S5 & S6);

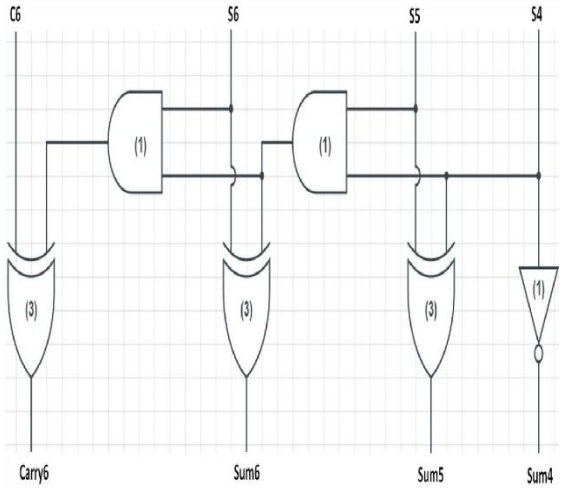

Fig 5: 4-bit BEC

IV. LINER BRENT KUNG CARRY SELECT ADDER

The CSLA consists of one multiplexer and two ripple carry adder in order to decrease the area and delay caused due to RCA[9], [10].The RCA with carry_in=0 is substituted by brunt kung adder (BK) Parallel prefix adder. Thediagram of LBKCSLA is shown below in the 16-bit LBKCSLA consists of four groups of same size with BKA for carry_in = 0 and RCA for carry_in =1. Now by using tree structure of BKA, the speed of addition operation is also increased.

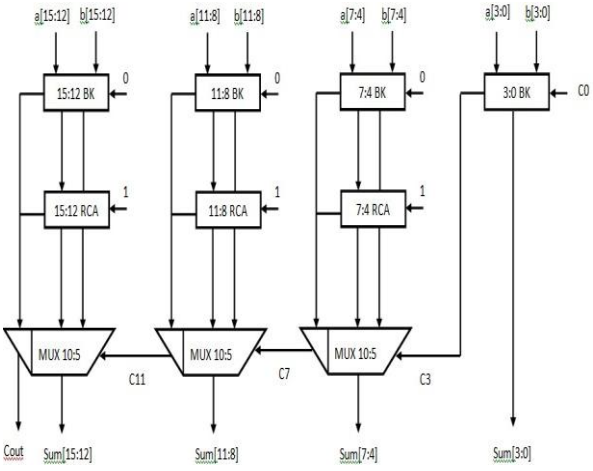

Fig 6 :LBKCSLA

V.SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

The delay[13] in LBKCSLA is again reduced by using square root structurethat contains 5 groups of size difference. Every group contains BKA for carry_in =0, RCA for carry_in =1 and having different multiplexer size thus this structure is know as SQRTBKCSLA. The SQRTBKCSLA block diagram is shown below

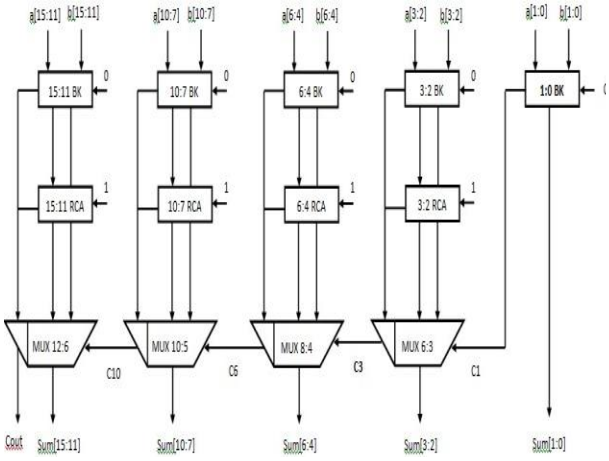

Fig 7 : SQRTBKCSLA

VI. MODIFIED SQUARE ROOT BRENT KUNG CSLA

In order to reduce the area , the ripple carry adder with carry_in =1 is replaced by BEC as the number of logic gates required for BEC is less than n-bit ripple carry adder thus this structure is know as MSQRTBKCSLA. The block diagram of 16-bit MSQRTBKCSLA is shown below

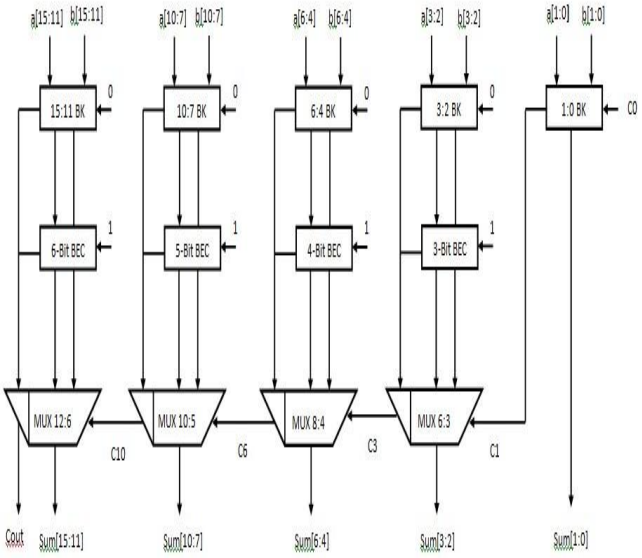

Fig 8 : MSQRTBKCSLA

The theoretically calculation can be done using AND, OR, Inverter(AOI) where the area and delay of MSQRTBKCSLA for each group are calculated

The values in the brackets in logic gates represents the particular gate delay

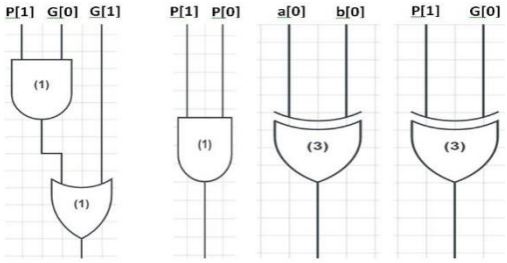

Fig a

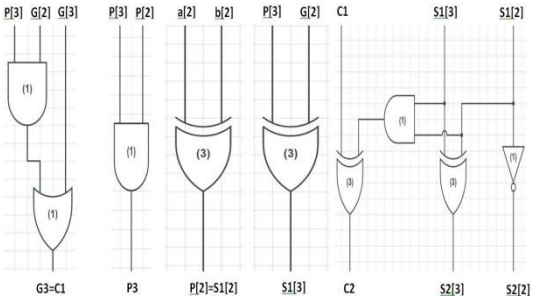

Fig b

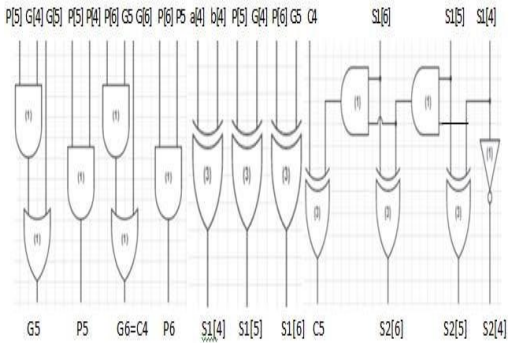

Fig c

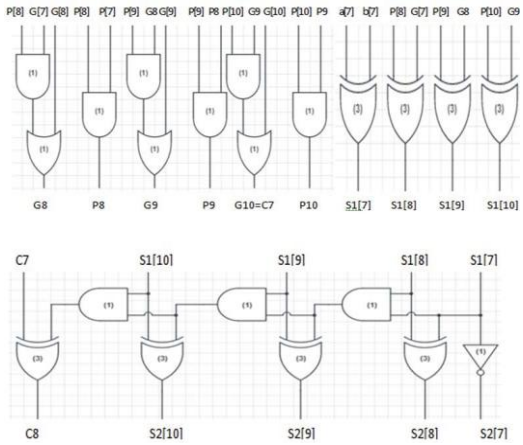

Fig d

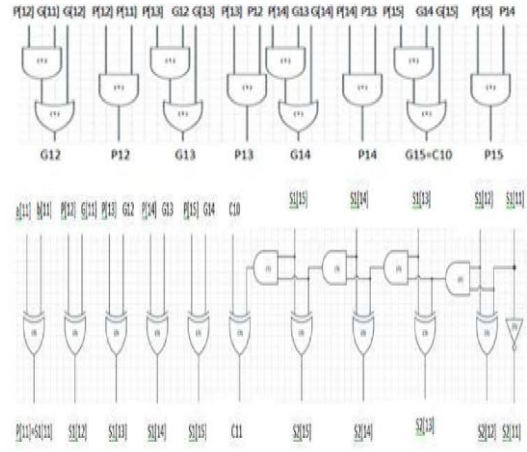

Fig e

The area and delay calculation of 16-bitMSQRTBKCSLA is projected by means of AOI logic as follows:

1.Group1 covers a 2-bit BKA. The delay of input signals P[0], P[1], G[0], G[1] generate signals) and area for P[0], P[1], G[0], G[1] is 5,5,1,1 (no. of gates) respectively.

2. Group2 contains a 2-bit BKA . The final summary and carry outputs of the Group2 such as S[2], S[3], Carry1 are obtained by applying the outputs to MUX unit. The delay is calculated in Group1. The delay for S[2], S[3], Carry1 is 8 units, 12 units and 13 units respectively.

3. Group3 comprises a 3-bit BKA and 4-bit BEC . The final summation and carry outputs of the Group3 such as S[4], S[5], S[6], Carry2 are obtained by put on the outputs to MUX unit.

4. Group4 contains a 4-bit BKA and 5-bit BEC . The final summation and carry outputs of the Group4 such as S[7], S[8], S[9], S[10],

Carry3 are gotten by spread on the outputs to MUX. The delay for S[7], S[8], S[9], S[10], Carry3 is 19 units, 19 units, 19 units, 19 units and 19 units respectively. Total area occupied by the Group4 is 92 (number of gates).

5. Group5 contains a 5-bit BKA and 6-bit BEC. The final summation and carry outputs of the Group5 as S[11], S[12], S[13], S[14], S[15], Cout are obtained by applying the outputs to MUX unit. The delay of Group5 is calculated as in Group1. The delay for S[11], S[12], S[13], S[14], S[15], Cout is 22 units, 22 units, 22 units, 22 units and 22 units respectively. Total area occupied by the Group5 is 92 (number of gates).

Similarly the area and delay evaluations for LBKCSLA and SQRTBKCSLA are also calculated and are tabulated in section VII.

VII.CHIP AREA AND DELAY EVALUATION

Table 1 : chip area evaluations of adders

Group no.	LBKCSLA Maximum Delay (units)	SQRTBKCSLA Maximum Delay (units)	MSQRTBK CSLA Maximum Delay (units)
1	10	6	6
2	15	11	13
3	17	13	16
4	20	16	19
5	--	19	22
Overall maximum delay	20	19	22

Table 2: Delay evaluation of adders

Group no.	LBKCSLA	SQRTBKCSLA	MSQRTBKCSLA
	Chip Area (No. of Gate Count)	Chip Area (No. of Gate Count)	Chip Area (No. of Gate Count)
1	48	20	20
2	120	58	44
3	120	89	68
4	120	120	92
5	--	151	116
Total Area	408	438	340

IX. CONCLUSION

Area and delay are calculated for LBKCLSA, SQRTBKCSLA and MSQRTBKCLSA and the comparison between all the three has also comprehensive. Finally it shows that the MSQRTBKCLSA has inhabiting less with somewhat increase in delay as associated to LBKCSLA and SQRTBKCLSA. As a results it finally concluded that modified square root brunt kung carry select adder (MSQRTBKCLSA) is improved compared to other two adders

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