# Design of Finfet Based Low Power Dynamic Comparator

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***Abstract***

*At current scenario, over power consumption becomes one of the major backlogs. In the design of cmos technology the short channel effect and leakage current may tends to become a vital drawback. In order to overcome this situation FINFET based dynamic comparator have been introduced, as it reduces the leakage and short channel effect. The main advantage of FINFET based dynamic comparator is that it provides 30% faster efficiency than CMOS.Dual input and dual output dynamic comparator is needed in high speed ADC application. In this project, a FINFET based low power dynamic comparator is designed with the help of tanner 13v tool. Its significant parameter is power consumption, delay, power delay product, which is being measured in a simultaneous manner.*

**Keywords**: *Dynamic comparator, FINFET,power consumption*

## I. INTRODUCTION

These Comparators have essential influence on theOverall performance in high speed analog to digital Convertors (ADCs).Comparator couldbea device that compares 2 voltages or currents and outputs a digital signal indicating that is larger. Its 2 analog input terminals V+ and V- and one binary digital output V0.
V0= {1, if V+ > V-

0, if V+ < V- }

Comparator are known as 1-bit analog to digital converter and that for reason they are principally used in large quantity in A/D device dynamic comparator are wide used in the design of high speed ADCs. Due to speed, low power consumption, dynamic latched comparator are very desirable for many applications like high speed ADCs, memory sense amplifiers(SAs) and knowledge receivers [1,2,3,4].The designed dynamic latch comparator is most widely used because it has many advantages such as high-speed, zero static-power consumption, high input impedance and full swing output. The main drawback of this comparator isProduced kick back noise[14,15].However, since this comparator has twotail transistors that limit the overall current flowing throughthe each of the outputs, it shows strong dependency of speedand offset voltage with different common-mode inputvoltage. To overcome this downside, the comparator withseparated input-gain stage and output-latch stage wasintroduced.

The structure of double-tail dynamic comparator isbased on design of a separate input and latch stage[15]. These separations allow quick operation over a large common-mode and providevoltage range. The conventional double-tail comparator doesn't need high voltage or stacking of too many transistors. A conventional double-tail comparator has less stacking and then can operate at lower supply voltages compared to the conventional dynamic comparator [8,12].

Dynamic comparator has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage, for fast latching independent of the input common-mode voltage (Vcm ), and a small current in the input stage , for low offset.

**[Dynamic = switching + short circuit (when the transistor is ON state)]**

Different circuit architecture can be proposed which avoids stacking of too many active/inactive transistors to supply rails to provide low voltage operation, as well as low static power consumption. Based on this principle, various architectures for dynamic comparator are proposed. Design presented in has high speed low power consumption, but it gives higher power consumption for smaller differential input voltage (less sensitive), low output swing for small

input differential voltage and gives highest power consumption for Vin=0. Design adopted by area and speed efficient but has excess power consumption. Conventional dynamic comparator has lesser transistor count among the all design and is also power efficient, but it requires higher supply voltage, also it is less sensitive and low speed. Many techniques are presented for low power design such as supply boosting methods, body driven transistor, current mode design and those with dual oxide processes [5, 6].

**Boosting Methods:**

Boosting and bootstrapping methods are used to increase the supply voltage, reference voltage, clock voltage and also avoiding the switching problems.

**Body Driven Transistor:**

These techniques remove the threshold voltage and body driven MOSFET suffer from lower Transconductance.

## II. PROPOSED FINFET BASED DYNAMIC COMPARATOR

FINFET technology has recently seen a serious increase inadoption for use within integrated circuits. The FinFETtechnology promises to supply the deliver superior levels of scalability required to Mack sure that the present progress withincreased levels of integration within integrated circuits canbe maintained. The FinFET offers many advantages in terms of IC process that mean that it's been adopted as amajor way forwards for incorporation within IC technology.

FinFETs is classified into two types: shorted-gate (SG) and independent-gate (IG). SG FinFETs are also called as three-terminal (3T) FinFETs and IG FinFETs as four-terminal (4T) FinFETs. In SG FinFETs, the front and back gates are physically shorted, whereas in IG FinFETs, both the gates are physically isolated. Thus, in SG FinFETs, shorted gates are jointly used to control the electrostatics of the channel. Hence, SG FinFETsshow higher on-current and also higher off-current compared to IG FinFETs.

### *A. FINFET based dynamic latch comparator*

The dynamic latch comparator is most widely used because it has many advantages such as high-speed, zero static-power consumption, high input-impedance and full swing output. The main drawback of this comparator is produced kick back noise.During the pre-charge phase both the output nodes are charged to power supply voltage and during the evaluation phase the outputof the comparator depends on the differential input. The main disadvantage of this comparator is it consistsof only 1 tail current semiconductor M11 that is used to control the currents flowing through boththe differential input pair (M10 and M5) and therefore the latch (M3,M4,M8,M9).During the pre-charge phase both the output nodes are changed to power supplyvoltage and during the evaluation phase the outputof the comparator depends on the differential input.

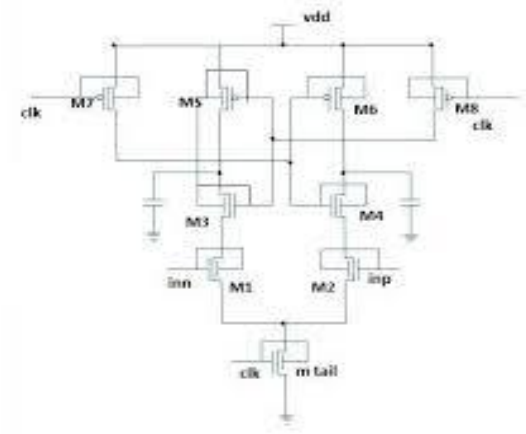


**Fig. 1FINFET based dynamic latch comparator**

The size of the tailtransistor M11 should be increased to increase thedrive currents of the latch. But, if we increase thesize of the tail semiconductor M11, the time length ofthe input transistors which operate in the saturation region will be reduced because the transistors operate less time in saturation region full amplification of input voltage is not achieved.

### *B. FINFET based Single tail comparator*

The Circuit diagram of the Single tail comparator. It is mostly used in A/D converters, with high input impedance, no static power dissipation and rail-to-rail output swing.The operation of the comparator can be explainedby using two Phases. When Clk=0, this circuit operates inreset phase. In this phase, Mtailtransistor get off and resettransistors (M7 and M8) pull each output nodes Outn andOutp to VDD to indicate a start condition and to have a validlogical level during this phase.

when CLK = VDD, thiscircuit operates as compared part, transistors M7 and M8are off, and Mtail is on. Outp, Outn which had been prechargedto VDD and start to discharge with differentdischarging rates depending on the corresponding inputvoltage (INN/INP).

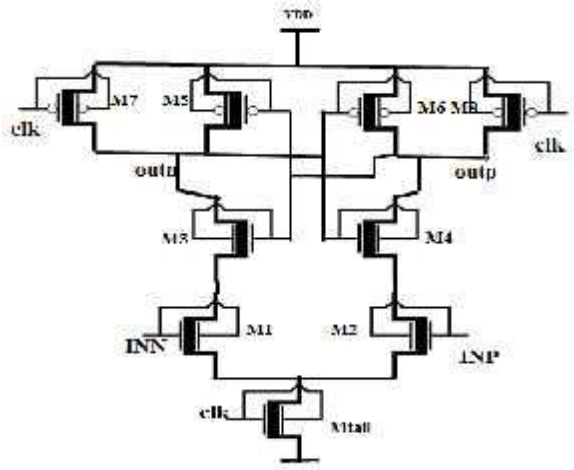


**Fig. 2 FINFET based Single tail comparator**

The total delay of single tail comparator is as follows
tdelay = t0 + tlatch
t0 represents the discharging delay
tlatch represents the latching delay.

This structure has the subsequent benefits like higherinput impedance, no static power consumption and rail-torailoutput swing. There are two drawbacks are presenting inthis circuits such as several stacking, due to the severalstacking high supply voltage is needed for its operation. Another drawback of this circuit is there is only one current path.

### *C. Conventional Dynamic Double Tail Comparator*

This design has advantage of low voltage Operation compared to dynamic comparator. It is named as double tail because, two transistors are attached at the end of supply rails to reduce static power consumption. Both tail transistors provide higher current in latching and regeneration phase to have high speed.

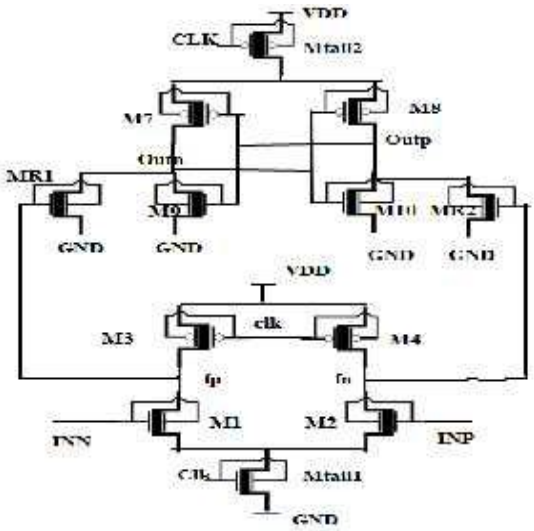


**Fig 3 FINFET based Conventional dynamic double tail comparator**

The operation of this comparator is as follows, when CLK = 0, this circuit operates in reset part. In this phase,Mtail1 and Mtail2 are off, transistors M3 and M4 prechargefn and fp nodes to VDD, that causes transistors MR1 and MR2 to discharge the output nodes to ground. In decision makingphase or comparison phase, CLK =VDD, Mtail1 andMtail2 gets on, M3 and M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by Mtail1current/Cfn(p) and on top of this, a ΔVfn(p) will build up.The intermediate stage formed by MR1 and MR2 passesΔVfn(p) to the cross coupled inverters. And conjointly provides a good shielding between input and output, resulting inreduction of kickback noise.

Apart from having advantage of low voltage operation, it is found that overall delay is reduced if ΔVin is increased. Thus delay of this comparator depends on input differential voltage as well as it requires higher supply voltage to compare smaller ΔVin.

Power consumption is based on two components as follows, Dynamic power dissipation - due to charging andDischarging of load capacitances (nodes) and shortCircuit current flow.Static power dissipation - due to sub-threshold leakage through OFF transistor, gate leakage throughGate dielectric and junction leakage from source/drain diffusion.

### *D. Proposed Dynamic Double Tail High Speed Comparator*

Schematic diagram of the proposeddynamic double-tail high speed comparator. Due to the better performance of double-tail architecture in low-voltagepurposes, the proposed comparator is designed based on thedouble-tail structure. The main idea of the proposed highspeed comparator is to increase ΔVfn/fp to increase the latchregeneration speed. For this reason, two control transistors(Mc1 and Mc2) are added to the primary stage in parallelto M3 or M4 transistors.

The operation of the proposed comparator is as follows, when CLK = 0, this circuit operates in reset phase. In this phase, Mtail1 and Mtail2 are off. It will be avoiding static power consumption. M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are gets off. Intermediate stage transistors (MR1 and MR2) reset both latch outputs to ground. In decision-making phase, CLK=VDD, Mtail1 and Mtail2 are gets on, transistors M3 and M4 turn off. Further at the beginning of this phase, the control transistors are still in off state.At the starting of the comparison phase or decisionmaking phase, due to the both fn and fp nodes have beenpre-charged to VDD. Both switches are in closed position and fn and fp being to drop with totally different discharging rates. As early as the comparator detects that one of the fn or fb nodes is discharging faster, control transistors will used hereto increase their voltage difference

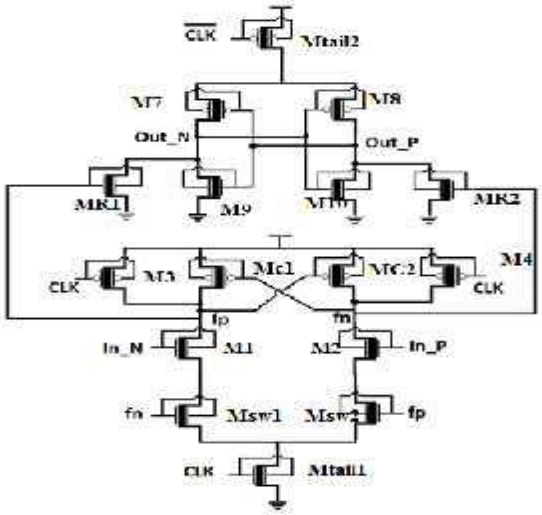


**Fig. 4 FINFET based proposed dynamic double tail high speed comparator**

Suppose that fn isincreasing up to the VDD and fp should be discharged fully, hence the switch in the charging path of fn will be opened toprevent any current drawn from VDD. But the other switchconnected to fp will be closed to allow the completedischarge of fn node. In another words, the operation of thecontrol transistors with the switches compete withsuccessfully the operation of the latch.

The analysis of proposed high speed comparator issimilar to the conventional double tail dynamic comparator, however; the proposed dynamic comparator enhances thespeed of the double-tail comparator by affecting twoimportant factors: 1st, it will increases the initial output voltage difference at the beginning of the regeneration and second, itenhances the effective transconductance of the latch.

## III. RESULTS AND SIMULATION

The FINFET based high speed comparator in 90nm can be designed in TANNER software. By using this software various parameters can be analysed. The transient analysis of 90nm outputs are

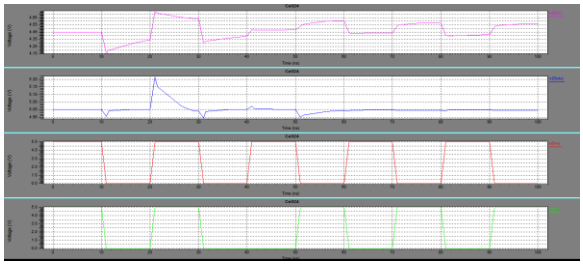

**Fig 5.aFINFET based dynamic latch comparator in 90nm**

FINFET based dynamic latch comparator is most widely used because it has many advantages such as high-speed, zero static-power consumption, high input impedance and full swing output. The main drawback of this comparator is Production of kick back noise.

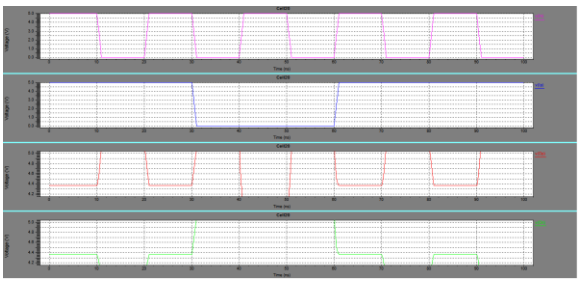

**Fig 5.b FINFET based Single tail comparator in 90nm**

FINFET based Single tail comparator such as higherinput impedance, no static power consumption and rail-to rail output swing. There are two drawbacks are present in this circuits such as several stacking,in which it needs high supply voltage as it is considered to be vital backlog.

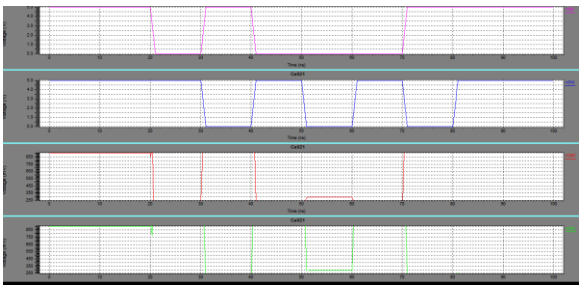

**Fig 5.c. FINFET based Conventional dynamic double tail comparator in 90nm**

FINFET based conventional dynamic double tail comparator gives less power consumption over single tail comparator. The intermediate stage formed by MR1 and MR2 passes ΔVfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduction of kickback noise.

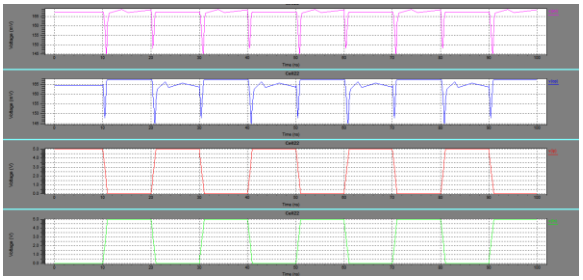

**Fig 5.d FINFET based proposed dynamic double tail high speed comparator in 90nm**

FINFET based proposed dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference at the beginning of the regeneration and second, it enhances the effective Trans conductance of the latch.

From the performance analysis it is understood that the 90nm structure has the lesser delay and the power consumption than the CMOS based 90nm structure. Morever it can operate at lower supply voltage than the 90nm CMOS devices.

**Table II : Parameter Analysis Of Finfet Based90nm Structre**

The analysis results of above simulation and its respective value are given in below tabular column

| PARA METER | Latch Dynamic comparator | Single tail dynamic comparator | Double tail dynamic comparator | Double tail Dynamic high speed comparator |
|---|---|---|---|---|
| Power (µw) | 2.14 | 1.27 | 2.12 | 1.02 |
| Delay (ns) | 4.09 | 3.09 | 1.35 | 1.27 |
| Power delay product (µw*ns) | 8.75 | 3.924 | 2.862 | 1.295 |

Table I describes the parameter analysis of FINFET based 90nm structure

Different types of comparator have been used. The most prominent and well known comparators have been used in the existing system.proposed system the power may corresponds to get reduced consequently.

## IV. CONCLUSION

In my previous study MOSFET based dynamic comparator has been recognized. Besides its merits it also has some drawback. In order to overcome this, FINFET is taken into consideration. The FINFET based High speed comparator in 90nm has been designed using simulation software. High speed can able to do here by the way of minimizing the delay. This work presents the delay analysis for clocked dynamic comparators. Two structures of Single tail comparator and conventional double- tail dynamic comparators are analyzed. A new high speed comparator with low-power capability has been achieved in order to improve the performance of the comparator and additionally reduces the delay.

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