Design of the Parity Preserving Reversible Gate Using Nano QCA

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Abstract

The improvements in the computer architecture has been the primary goal of the researchers and designers since new model have made their way. One of the emerging architectures that have made its ground as research area is the concept of reversible logics. Reversible logic suggest the system with zero heat dissipation . It satisfies the work and heat relations according to quantum mechanical effect and coulomb's law.In this paper a reversible gate called parity preserving gate has been designed using QCA technology. The parity preserving reversible gate enables rich fault tolerance features as well as reversibility attributes. It is used in the ALU of processors for higher fault tolerance. The design is verified by comparing the simulation outcome with theortical values. The proposed model is evaluated and simulated using QCADesigner tool version 2.0.3.

Keywords - *Quantum dot Cellular Automata(QCA) , Reversible logic , parity preserving gate , QCADesigner.*

I.INTRODUCTION

In nano scale logic design a power consumption is the most challenging area.Hence, there is a raising requirement for a new technology that can provide nano size circuits having lesser power dissipation.QCA offers high device density, low power consumption and high switching speed.[7],[8].Due to these properties quantum gates have been targeted for their enabling roles towards computational reversibility. The limitation of heat dissipation of the computing systems is the main driving force which draws the attention of reversibility. Reversible logic conserves the information which is analogous to conservation of energy and momentum in physics. The inherent of reversibility lead a new frame work that results in zero heat dissipation. Reversibilty in QCA is one to one mapping of inputs to outputs.In 1961,Landau suggested that the loss of one bit of information expense greater than are equal to KTln2 joules of energy[21]. This suggests the system which are irreversible do not conserve information and are lossy.Further to strength the theortical concept Bennet derived some important analysis[24][5].Bennet clock mechanism achieves less than KTln2 switching energy dissipation[2][11].Reversibilty is a notion which calls for bijective function.It suggest that a backward and forward track both are possible at any time for a system. While designing reversible logic circuits mapping should be taken care as fanout is not allowed.The list of contribution is as follows.

- The building blocks of a reversible system should be individually reversible.
- The number of inputs and outputs has to be always equal.

The emerging concept of reversibility attracts the VLSI designer since CMOS is suffering the issue of power dissipation at nano scale levels[6].The new design if successfully used in designing reversible circuits can lead to ultra low power systems. In this paper a new qca implementation of parity preserving reversible gate is designed using cell minimization techniques.

II BACKGROUND

A. QCA Review

In order to overcome the problem of size reduction in CMOS technology ,Craig Lent and Al introduced a new paradigm of the architecture of calculation called Quantum dot Cellular Automata. QCA cells have been realized through several physical implementations, of those implementation methods semiconductor and metal island are the most promising ones due to their high operation and integration density[9].

This QCA technology composed of array of cells in each one there are four quantum dots.The electrons occupy two diametrically opposed quantum dots.There are two stages of polarization that corresponds to the electrons.When the electrons are in lower left and higher right the polarization is P=+1 and when it is in the lower right and higher left the polarization P=-1.The planar crossings can also be obtained by using a turned version 450 of a cell.

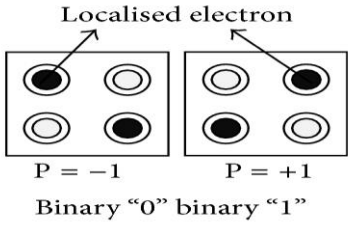


Fig.1 QCA cell with four quantum dots

The logical information can propagate from the input to the output of the cell by the force of repulsion. The fundamental QCA logic primitives are QCA wire, QCA inverter and QCA majority gate. The binary signal propagates from input to output because of electrostatic interactions.90° and 45° QCA wires can be used.The QCA inverter is created by orienting the cells at 45 ° to each other to take opposite polarizations[20],[22].

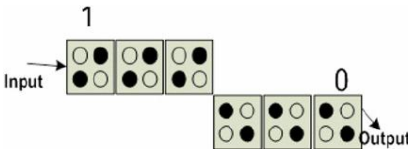


Fig.2 QCA inverter

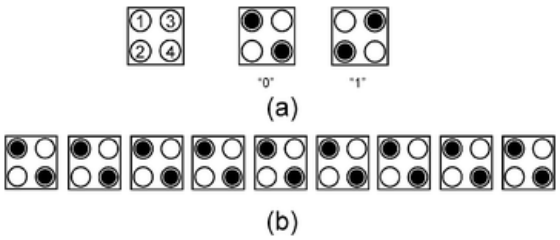


Fig.3 QCA wire

B.QCA Clocking

Synchronization and energy restoration are essential for the proper propagation of QCA signal. Those can be obtained by applying specific four phased clocking scheme. There are two types of clocking proposed by Launder and Bennet. The Launder clocking scheme is generally used in circuits. It has four distinct zones switch ,hold, release and relax where each zone is shifted by 90° compared the previous zone[15],[16].The clocking statergies in conjuction with design statergies can lead to the concept of physical reversibility.More over each QCA clock zone consist of atleast two cells to preserve the influence on clock zone.

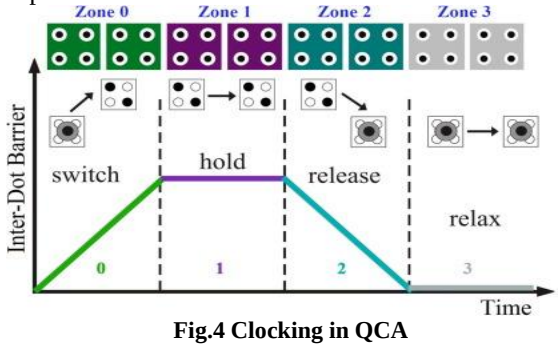


Fig.4 Clocking in QCA

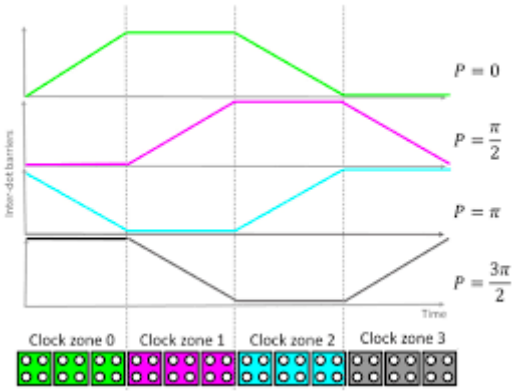


Fig.5 Clock phase shift in QCA

TABLE I. Operation of QCA clock pulses

Clock pulse	Potential Barrier	Polarization state of the cells
Hold	Held High	Polarized
Switch	Low to High	Polarized
Relax	Low	Polarized
Release	Lowered	Polarized

C.Reversible Computing

Certain amount of energy is wasted when the input bits are destroyed. Reversible logic circuits, avoid energy waste by recovering the energy into the system. Bennet proposed that very low power consumption is possible in logic circuits when it is combined with logic gates[23]. A gate is reversible if each one of the distinct input have distinct output. One of the advantages of the reversible gates is that they are balanced. A circuit combined the reversible gate with no constant inputs satisfies the balance functions[12]. Garbage outputs can be used to satisfy the non balanced functions. Reversible computation analyze the ratio between consumed energy and logical computation. It can be established at logical level by one to one layout between input and output of the circuits[17],[18].

To prevent the destruction of data bits during logical operation, they are designed to reduce power consumption. The data bits in reversible computation are preserved that lead to the development of reversible gate[13].

The reversible gate should have the following characteristics ,

- Minimum garbage outputs.
- Minimum input constants.
- Minimum area.
- Minimum number of gates.

Several reversible gates have been developed.Two important types are Toffoli and Fredklin gate[10].

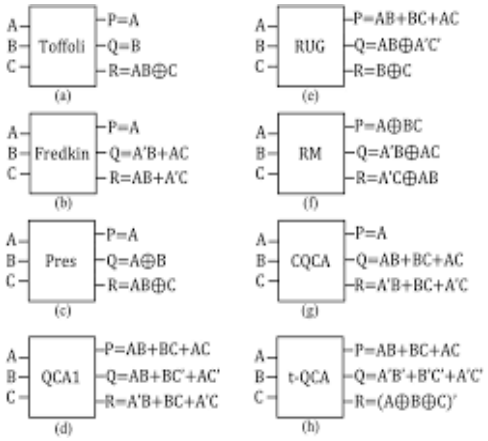
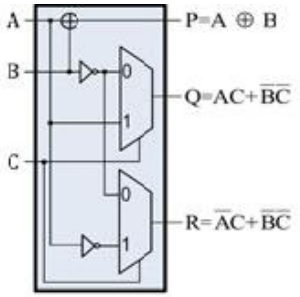


Fig.6 Reversible gates

Parity Preserving Gate

Parity preserving reversible logic gates are the class of reversible logic gate with additional property which is the parity of input is same as that of output.[1]

This proposed design of Parity Preserving Reversible Gate(PPRG) is designed using multiplexers and Ex-or gate[14].It provide one to one mapping of input and outputs[4].Hence the input signal could be extracted by knowing the output.This validates the reversible property.



A	B	C	P	Q	R
0	0	0	0	1	1
0	0	1	0	0	1
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	1	0

Fig.7 Parity Preserving Reversible gate

The fig.8 shows the circuit and its related truth table of PPRG.The output include P=A⊕B,Q=AC+ $\bar{B}\,\bar{C}$,R= $\bar{A}C$+ $\bar{B}\,\bar{C}$,here A,B,C are the inputs[19].

The design satisfies the reversible gate parity preserving capabilities.They are

- Mapping of input to output is bijective.
- Ex-OR of input produces a result equal to Ex-OR of outputs.

Proposed Parity Preserving Reversible Gate[Pprg]

The proposed gate design provides equal parity for each input set and corresponding output set.

Here the new QCA implementation of the PPRG is proposed using cell minimization techniques. The techniques are

- The minimum distance between the adjacent rows of cells is the width of two cells.
- The minimum distance between the adjacent columns of cells is the width of two cells.
- Directly the output and polarizations are fixed in multiplexers and ex-or instead of using extra cells.
- To reduce the area of gate the multiplexers and ex-or gate are aligned one below the other.

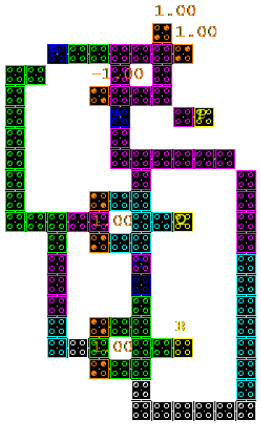


Fig.8 Quantum representation of PPRG

IV.RESULT AND DISCUSSION

A. Simulation Parameters

The design implementation and simulation is achieved through QCADesigner 2.0.3[24],[25].The bistable simulation is carried out with 18X18 nm QCA cell.

B.Simulation output of PPRG

The simulation result of the proposed Parity Preserving Reversible Gate is shown in the Fig.10 and the result is compared with the truth table. From Fig.9 shows the input sequence {A,B,C} is {1,1,1}produces the output sequence {P,Q,R} is {0,1,0}.(i.e) when A=1; B=1; C=1; P=A⊕B=0; Q=AC+ $\bar{B}\,\bar{C}$=1; R= $\bar{A}C$+ $\bar{B}\,\bar{C}$ = 0

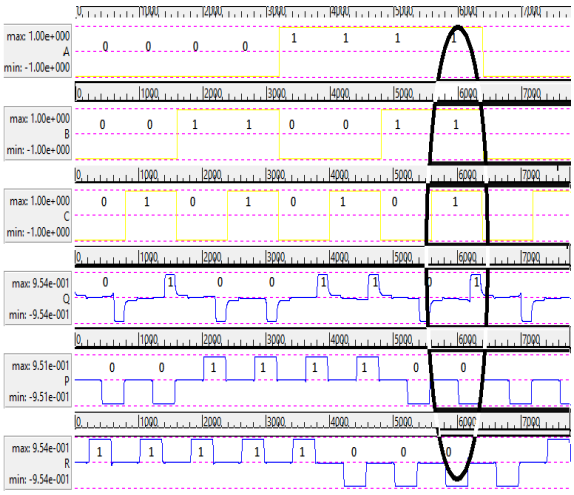


Fig.9 Simulation output of PPRG

TABLE II Performance analysis

	Circuit	Cell count	Cell area(μm^2)	Latency
PPRG[1]	Ex-Or	30	9720	3.75
	Mux	48	15552	
	PPRG	170	55080	
Proposed PPRG	Ex-Or	15	4860	3
	Mux	12	3888	
	PPRG	83	26892	

V.CONCLUSION

Energy conserving gate designs allow extension in beneficial direction by embracing reversibility.The PPRG with new QCA implementation has been designed and implemented.The functionality of the circuit is tested and verified using QCA Designer 2.0.3. The performance analysis of the proposed circuit were compared with the previous design .The number of cells and area in QCA layouts are lower compare with the existing design.

In future work the building blocks of ALU and even other circuit like multipliers,shifters etc can be implemented using reversible logic circuits and it can be used in many application in the area of communication for enabling the storage.

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