Design of Optimized QCA Sequential Circuits

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Abstract

The scenario of the digital industry has changed in the past few years due to the rapid development of technology.Among several other alternatives,QCA is the innovative technology to design digital logic circuits using quantum dots confined in the potential well. This paper proposes the optimum design of sequential circuits like flip-flops and shift register by using majority gates and is implemented by cell minimization technique. It will reduce the area and complexity. The functionality of the circuits can be tested by using QCADesigner version 2.0.3.

Keywords - *Quantum-dot cellular automata ,sequential circuit, flip-flops, shift register,QCADesigner.*

I.INTRODUTION

To making the small transistor,It is great advancement in electronics and computer industry over the past 60 years.In CMOS the serious effects due to physical barriers such as short channel effect,leakage current and excessive power dissipation at nanoscale regions.Hence one possible alternative method is QCA to overcome this problem.QCAtechnologytransfer's information by means of polarization using the flow of electrical current.It provides ultrasmallfactor,low power consumption and high speed clock circuits.

A sequential circuit is a type of digital circuit whose the output depends on the present value of the input signal as well as the sequence of past inputs.

Types of sequential circuit:

1. Synchronous circuit:It uses the clock input to derive the circuit.
2.Asynchronous circuit:It doesn't uses the clock signal to drive the circuit.

QCA is the new paradigm that performs computation and routing information at Nano domain.The advantage of QCA over the CMOS is lesser delay, high density circuit and low power consumption.

II.REVIEW OF QCA

The logic states are the unique feature of the QCA and it is represented by a cell. QCA cell contain four quantum dots arranged in corners of the square.Then two electrons are used to provide a tunneling between these two dots.The polarized charge can transferred by the columbic repulsion within the square cells.

A basic QCA cell consists of four quantum dots in square array.

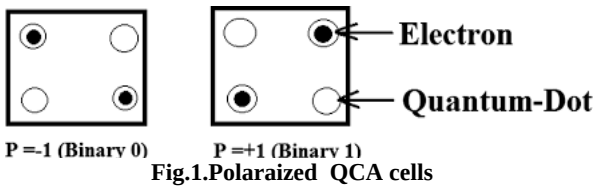

Fig.1.Polaraized QCA cells

Polarization p=-1and p=+1 represethe logic states 0 and 1.To perform logic funtion invertor and majority gate are needed. In QCA logic values are stored based on electron's charge rather than electrical pulse like in CMOS.

The automatic logic synthesis for QCA circuit s hasthe different aspects.

The functional level:It is used to describing and generating a connectivity of the circuit to be realized.

The physical level:It is used to describing and evaluating the cost a circuit interms of area,delay and energy dissipation.

The geometric level:It is used to describing and generating the layout out QCA circuit.

III.BASIC QCA ELEMENTS

A.QCA WIRE

The binary signal propagates from input to output because of the electrostatic interaction between cells. Moreover in a QCA wire, all the computational power is provided by the coulomb interaction between cells and there is no electrical current flow between cells and hence no power dissipation.

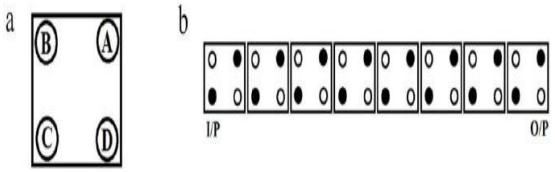

Fig.2.QCA Wire

B.QCA WIRE-CROSSING

In QCA, two kinds of QCA wire-crossing are possible-coplanar and multilayer. Coplanar wire crossing in QCA requires cells of two different orientations, a 90 degree and a 45 degree structure

whereas multilayer wire crossing has no such strict orientations constrain. The crosstalk between the coplanar crossing can be avoided by introducing multilayer wire crossing.

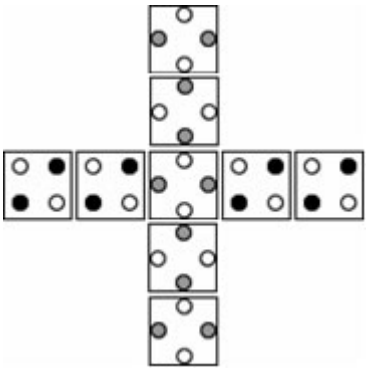

Fig.3.QCA Wire Crossing

C.QCA MAJORITY GATE

The governing equation for the majority gate is,M(a;b;c)=ab+bc+ca.

Two input ANDandOR gates can be implemented with three input majority gates by setting one input to a constant with ANDs,ORs and Inverters,any logic function can be realized.

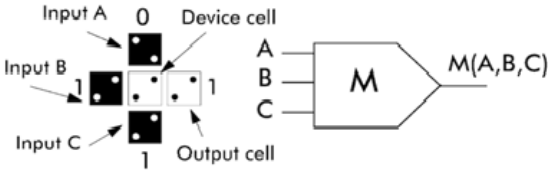

Fig.4.QCA Majority Gate

TABLE I.Truth table of majority gate

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

D.QCA INVERTER

Two standard cells in a diagonal orientation are geometrically similar to two rotated cells in ahorizontal orientation.For this reason, standard cells in a diagonal orientation tend to align in opposite polarization directions as in the inverter chain.

The signal comes in from the left, splits into two parallel wires and is inverted at the point of convergence.An inverter gate can be implemented using 11 new proposed QCA cells.

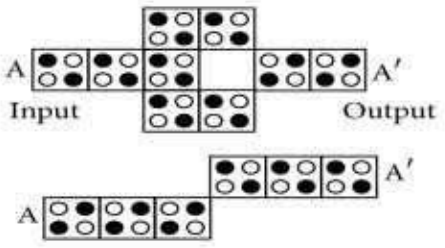

Fig.5.QCA Inverter

E.QCA Clocks

The circuit area is divided into four sections and they are driven by four phase clock signals.As shown in figure,there is a 90 degree phase shift from one section to the next.In each clock zone,the clock signal has four states:high-to-low,low-to-high and high.The cell begins computing during the high-to-low state and holds the value during the low state. When the clock is in the low-to-high state,the cell become released and inactive during the high state.

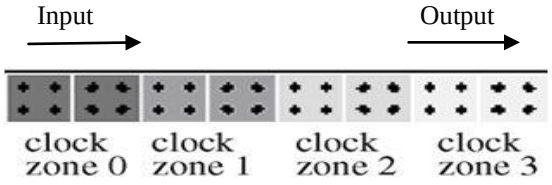

Fig.6.QCA Clock

The QCA clocking signal is used to control the signal propagation along the QCA cells arrangement.Then it is also used to synchronize the digital circuits.

There are four-different clocking phases such as,SWITCH,HOLD,RELEASE and RELAX.

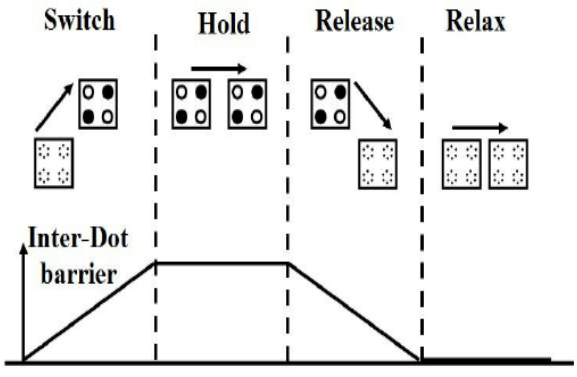

Fig.7.Four phases of clocking

SWITCH:During this phase,the inter-dot barriers are slowly raised and the computation takes place according to QCA cell arrangement.

HOLD:In this phase,the inter-dot barriers are kept high and the QCA cells retain their states.

RELEASE:The barriers are lowered and the cells are allowed to relax to unpolarized states during release phase.

RELAX:In this phase, the barriers are kept low and the cells remain in unpolarized state.

IV.CELL MINIMIZATION TECHNIQUE

The proposed design based on cell minimization technique used for reducing the majority gate.

1.The number of majority gate is connected spontaneously without using extra cells.

2.To reduce the length of the circuit the majority gates are aligned in parallel manner.

3.Directly the output and polarization are fixed in majority gates instead of using extra cells.

V .PROPOSED DESIGN OF FLIP-FLOPS

Flip-flop is a one bit storage device and it is the sequential circuit, whose output is depend on the present input as well as past output.Then the types are given below

SR flip-flop,Dflip-flop,JK flip-flop,Tflip-flop.

S.No	PARAMETERS	EXISTING SYSTEM[1]	PROPOSED SYSTEM
1	Complexity	38	14
2	Area	0.04μm^2	0.012 μm^2
3	Latency	1.5	1
4	Majority gate	4	1

A.QCA Based Sr Flipflop Design

The SR flip-flop has two data inputs S and R. The S input is made high to store 1 in the flip-flop and R input is made high to store 0 in the flip-flop. In this when both inputs are same then the output either does not change or it is invalid.

TABLE II.Characteristic table of SR flip-flop

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	Intermediate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Intermediate

Characteristic equation of SR flip-flop:

$$Q_{(t+1)}=S+R'Q$$

The majority gate implementation of SR flip-flop has 1 majority gates and 3 inverters. In this S input is complement with the R input. The outcome of M1 is complemented and feedback to the S input .The output obtained by M1 is complemented to produce output Q0.

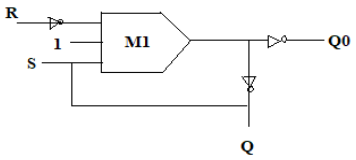

Fig.8 SR Flip flop design using Majority gate

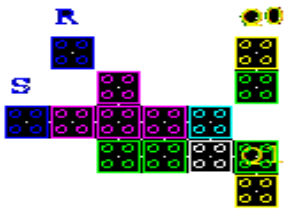

Fig.9 QCA cell layout of SR Flip flop

TABLE III.PERFORMANCE COMPARISION

B.QCA Based Jk Flip Flop Design

Inputs J and K behave like input S and R to set and clear the flip-flop(the letter J is for set and the letter K is for clear). When logic 1 input is applied to both J and K simultaneously, the flip-flop switches to its complement state, i.e., if Q=1, it switches to Q=0 and vice versa. The output Q is AND with K and clock pulse only if Q is previously 1.similarly, output Q' is AND with J and clock pulse only if Q was previously 1. The behavior of JK flip flop is demonstrated in the characteristic table.

Characteristic Equation of JK Flip Flop:

$$Q(t+1)=JQ'+K'Q$$

TABLE IV.Characteristic table of JK Flip Flop

Q	J	K	Q_{t+1}
0	**0**	**0**	**0**
0	**0**	**1**	**0**
0	**1**	**0**	**1**
0	**1**	**1**	**1**
1	**0**	**0**	**1**
1	**0**	**1**	**0**
1	**1**	**0**	**1**
1	**1**	**1**	**0**

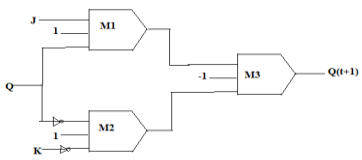

Fig.10JK flip flop design using majority gate

The majority gate implementation of JK flip flop has 3 majority gates and 2 inverters. Input to M1 is J and Q, input to M2 is K' and Q'(complement of Q input given in M1). The output of M1 and M2 is given as a input to M3 which produces the output JQ'+K'Q.

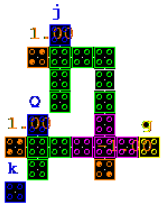

Fig.11QCA cell layout of JK Flip-Flop

TABLE V. Performance Comparison

S.No	PARAMETERS	EXISTING SYSTEM[1]	PROPOSED SYSTEM
1	Complexity	78	21
2	Area	0.071 μm^2	0.03 μm^2
3	Latency	1.5	1
4	Majority gate	6	3

C.QCA Based D Flip Flop Design

The D flip flop is a modification of the clocked SR flip flop. It has two inputs: D and Clock.In D flip flop,the next state is always equal to the D input and it is independent of the present state.Therefore,D must be zero if Q t+1 have to be 0 and 1 if Q t+1 have to be 1,regardless of the value of Q.

TABLE VI.Characteristic table of D Flip Flop

Q	D	Q t+1
0	0	0
0	1	1
1	0	0
1	1	1

Characteristic Equation of D Flip Flop:

$$Q_{(t+1)}=D$$

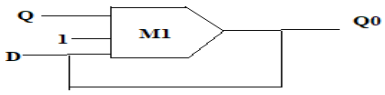

Fig.12D Flip Flop design using majority gate

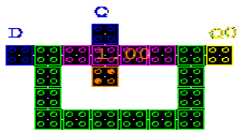

Fig.13QCA Cell Layout of D-FF

The majority gate implementation of D flip flop has 1 majority gate.The input for M1 is D and Q . The output(Q0) is feedback to D to produce the result Q=D.

TABLE VI. Performance Comparison

S.No	PARAMETERS	EXISTING SYSTEM[1]	PROPOSED SYSTEM
1	Complexity	43	20
2	Area	0.04 μm^2	0.02 μm^2
3	Latency	1.25	1
4	Majority gate	4	1

D.QCA Based T Flip Flop Design

T flip-flop is also known as the Toggle flip-flop. The T flip-flop is a modification of JK flip-flop.

TABLE VII.Characteristic table of T Flip Flop

Q	T	Q (t+1)
0	0	0
0	1	1
1	0	1
1	1	0

The sscharacteristic table and the characteristic equation shows that when T=1,the state of the flip-flop is complemented; when T=0,the state of the flip-flop remains unchanged. Therefore, for 0-0 and 1-1 transitions T must be zero and for 0-1 and 1-0 transitions T must be 1.

Characteristic Equation of T flip-flopQ(t+1)=TQ'+T'Q

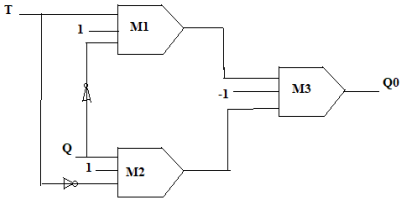

Fig.14 T Flip Flop design using majority gate

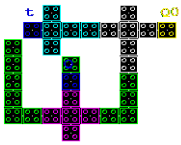

Fig.15QCA cell layout of T Flip Flop

The majority gate implementation of T flip flop requires 3 majority gate.It is similar to that of JK flip flop.In T flip-flop,the input givetn to M1 is inverted and given as a input for M2. The outcome of M1 and M2 is given as a input to M3 which produces the result Q0=TQ'+T'Q.

E. PROPOSED DESIGN OF SHIFT REGISTERS

Shift register is a digital memory.Bits enter the shift register at one end and emerging from other end. The two ends are called as left and right. Hence the shift register is abidirectional FIFO circuit.Its commonly used in convertors that translate parallel to serial data,or vice-versa.It is also function as delay circuit and digital pulse encoders.

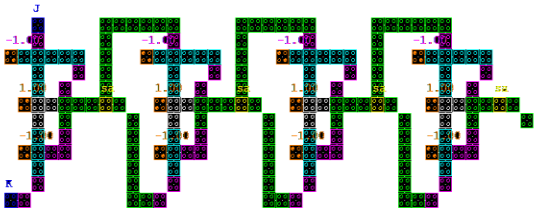

Fig 16.QCA cell layout of shift register using jk Flip-Flop

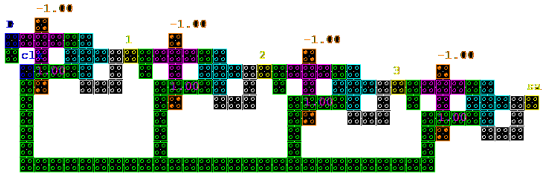

Fig 17.QCA cell layout of shift register using D Flip-Flop

A shift register is a cascade of Flip-Flop,sharing the same clock,in which the output of each Flip-Flop is connected to the data input of the next Flip-Flop in the chain. Shift register is a multi-dimensional,hence it is implemented simply by running several shift registers of the same bit length in parallel.

TABLE VIII.Performance comparision of Shift register using JK flip-flop:

s.no	Parameters	Existing system [2]	Proposed system
1	Cell count	238	173
2	Area	0.20μm^2	0.16μm^2
3	Latency	1	1
4	Quantum cost	238	173

TABLE IX.Performance comparision of shift register using D flip-flop

s.no	Parameters	Existing system[22]	Proposed system
1	Cell count	256	138
2	Area	0.20μm^2	0.14μm^2
3	Latency	4	4
4	Quantum cost	256	138

VI.RESULTS AND DISCUSSION

A.Simulation parameters

The design implementation and simulation is achieved through QCADesigner 2.0.3. The bistable simulation is carried with 18X18 nm QCA cell.

B.Simulation Output of Sequential circuits

The simulation result of the proposed sequential circuit is shown in Fig 18-23 and the verified with its truth table.

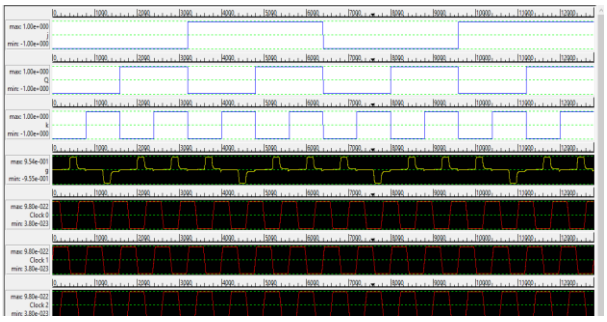

Fig.18 Simulation result of SR Flip-Flop.

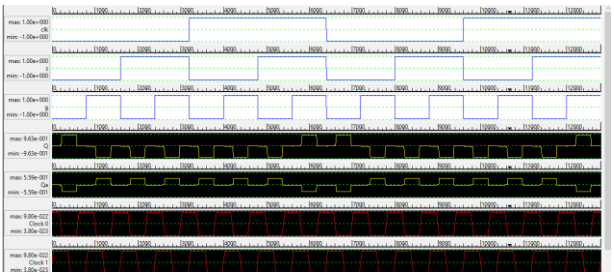

Fig. 19 Simulation result of JK Flip-Flop.

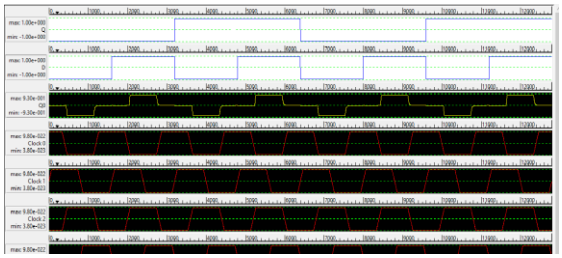

Fig.20 Simulation result of D Flip-Flop

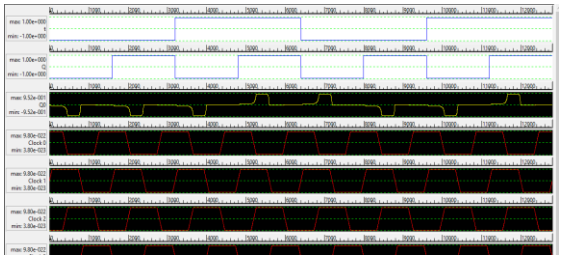

Fig. 21Simulation result of T Flip-Flop

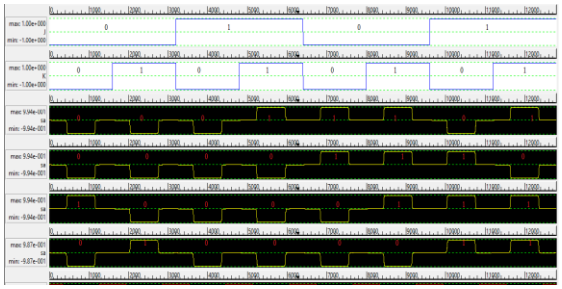

Fig. 22 Simulation result of Shift register using JK Flip-flop

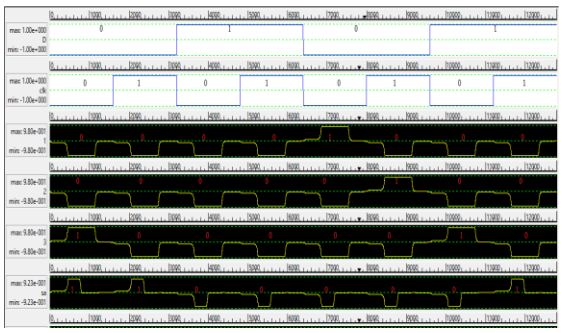

Fig.23 Simulation result of Shift register using D flip-flop

VII.CONCLUSION

In this paper, the optimized sequential circuits like flip-flop and shift register has been designed. The designed flip-flops with less complexity that has been used for the design of Shift registers. The QCA layout designs have minimum cell count and area leading to optimum design . The functionality of the different flip-flops, shift registers are verified using QCADesigner 2.0.3.

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