Self Checking TMR Voter with Optimized Pattern Generation

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Abstract

Self-repairing circuit is organized with building blocks that have identical structures to replace a faulty module. Propose a minimum switching activity pattern generation technique for triple modular redundancy(TMR) system.The original block is replicated thrice all three blocks receive the same inputs and a majority two out of three voter is used to determine the correct result. In this testing process group based selection algorithm is employed for the scan chain reorder in order to improve the fault coverage. In this methodology geffe generator and smoother is used in the pattern generation technique to identify the correct pattern and the smoother is the process of filtering the module. In this mode use a EX-OR gate for the repetition of the sequence is avoided and this gate is act as the comparator and the geffe generator is used to select the one of the three working module by using this generator low power dissipation and switching activity is reduced..We also propose a new, very effective compression scheme based on LUT access in order to reduce switching activity .The utilized technique is specified by taking into account the occurrence frequency of multiple kinds of information. The objective is to produce Test Pattern with good randomness; then fault coverage will be better. Fault simulation is done using xilnx simulator

I. INTRODUCTION

In recent years, circuit size has increased due to scaling down of technology. Controlling power dissipation in these large circuits during test sessions is one of the major concerns in VLSI testing. In general power dissipation of a system in test mode is higher than the normal mode. The power consumption of the chip during manufacturing test can be significantly higher than the power consumption of the chip in its target system. This increase in the power consumption can be attributed primarily to on-chip extremely random test pattern generation. This extra power can cause problems such as instantaneous power surge that causes circuit damage, formation of hot spots, difficulty in performance verification and reduction of system lifetime and product yield [8]. The reason behind the high power dissipation during test is because unlike normal mode operation of the system correlation between consecutive test patterns does not exist in test mode. This is particularly true in case of Built-In-Self-Test (BIST), a popular DFT methodology. To increase the correlation between consecutive vectors during testing, several techniques have been proposed for creating low transition density in the pattern sets and thus control the power dissipation. However, this in turn increases the test application time as the test has to run for longer test sessions to reach sufficient fault coverage. Increase in test time is undesirable as testing cost of a chip is directly related to the time it takes to test the chip.

Built in self test (BIST) As the complexity of modern chips increases, external testing with Automatic Test Equipment (ATE) becomes extremely expensive. Instead, built-in self-test (BIST) is becoming more common in the testing of digital VLSI circuits since it overcomes the problems of external testing using ATE. BIST test patterns are generated internally using some some parts of the circuit, also the responses are analyzed using other parts of the circuit. When the circuit is in test mode, test patterns generators (TPG's) generate patterns that are applied to the CUT, while the signature analyzer (SA) evaluates the CUT responses. One of the most common TPG is the (linear feedback shift register) LFSR [6]. LFSR's are used as TPG's for BIST circuits because, with little overhead in hardware area, a normal register can be configured to work as a test generator, and with an appropriate choice of the location of the XOR gates, the LFSR can generate all possible output test vectors (with the exception of the 0s-vector, since this will lock the LFSR). The pseudorandom properties of LFSR's lead to high fault coverage when a set of test vectors is applied to the CUT compared with the fault coverage obtained using normal counters as TPG's. Logic built-in selftest (LBIST) is well known as one of the technologies to reduce test data volume. In general, LBIST uses pseudorandom pattern generator (PRPG) with high switching activity. Therefore LBIST makes high power consumption during scan shift operation. As the results,

it increases test time (costs) because test engineer has to slow down shift speed to solve power issue [4]

II. AUTOMATIC TEST PATTERN GENERATION (ATPG)

The automatic test pattern generator (ATPG) is software dedicated to the generation of test vectors that are used to detect the modeled faults in a CUT. Since in many cases the generated vectors do not achieve 100% fault coverage, the ATPG gives statistics about the FC achieved, the percentage of redundant faults, and the aborted faults which will therefore not be detected) for these test vectors. ATPG tools can be divided into two types: combinational ATPG and sequential ATPG. The combinational ATPG is dedicated to generating test sets for combinational circuits, or scan-based sequential circuits where all of the state elements can be accessed directly through the scan-chain.

III. LOW POWER TEST PATTERN GENERATION

With the development of portable devices and wireless communication systems, design for low power has become an important issue. Minimising power dissipation in VLSI circuits increases the battery lifetime and the reliability of the circuit. In general, the power dissipation of complementary metal oxide semiconductors (CMOS) circuits can be divided into two main categories: static power and dynamic power [1]. Static power is the power dissipated by a gate when it is not switching. A significant fraction of static power is caused by the reduced threshold voltage used in modern CMOS technology that prevents the gate from completely turning off, thus causing source to drain leakage. All the components of static power dissipation have a minor contribution to the total power dissipation, and can be minimised for well-designed circuits. On the other hand, dynamic power dissipation, which is the dominant source of power dissipation in CMOS circuits, occurs while the circuit is switching. The circuit is active when the applied voltage to an input of a cell changes, resulting in a logic transition in one or more outputs of the circuit at transistor level [3 9]. Hence, charging discharging of the load capacitances of transistors is the main source of dynamic power dissipation

IV. EXISTING SCHEMES

Abu-Issapresents a weighted based cell segmentation algorithm for multiple scan-chains BIST in order to reduce the average power consumption during the scan in of new test vectors, and to reduce the test application time. This technique is based on selecting the best group of cells to be connected in the same scan-chain. This group of cells should have the same or very close weight of logic 1's and 0's that will be optimal to get the highest fault coverage in a specified test length. Then each scan chain input will be connected to an output of a combinational circuit located after the Linear Feedback Shift Register that will generate biased test vectors according to the optimal weight of this segment of cells in the scan-chain. Thus, increasing the fault coverage and smoothing the applied test patterns which will reduce the power consumption.

This design is divided into two main stages: The first stage is to find the weight of logic 1 and logic 0 for each cell in the scan chain, while the second stage works in dividing the scan-chain into multiple segments such that each segment will include the scan cells that have approximately the same weight.

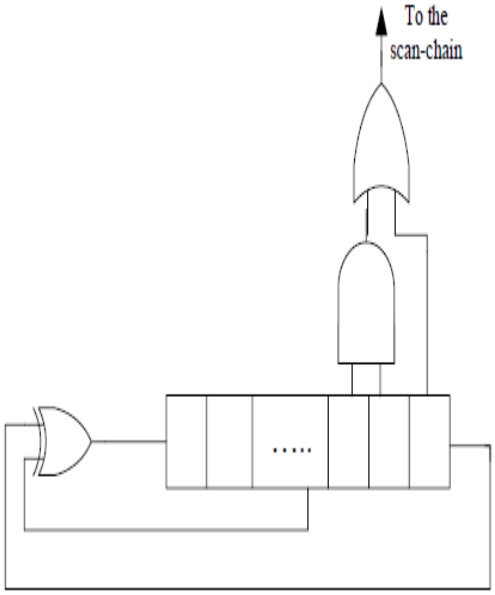

Fig. 3.1 Weight biased combinational circuit used to feed the scan-chain

Fig 3.1 shows a circuit that will scan-in biased test vectors in a weight very close to the above percentage (the circuit is taken directly from any simple truth table that has an approximate weight of logic 1 and logic 0 as specified by the weights above). In this way, we will not only get high fault coverage in shorter test length, but also we will reduce the number of transitions while scanning in the test vectors since the test vectors will be smoother due to their bias to certain logic value.

V. PROPOSED SYSTEM

In this project propose a testing methodology for the scan-based BIST. A smoother and geffe generator is included in the test pattern generator (TPG) to reduce average power consumption during scan testing, while a

group-based selection algorithm is employed for the scan-chain reorder in order to improve the fault coverage Segmentation by geffe generator

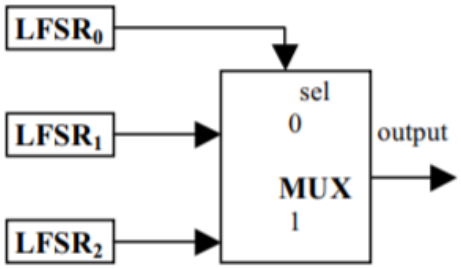

Figure 1. Conventional Geffe Generator

Proposed methods comprises three LFSMs and a 2-to1 multiplexer. A common choice for these LFSMs is the LFSRs which can achieve maximum cycle length (i.e. LFSRs which can be described by a primitive polynomial). Proposed system which makes use of three LFSRs: LFSR0, LFSR1, and LFSR2 . The bit generated by LFSR0 selects either LFSR1 or LFSR2, and the corresponding bit from the selectedLFSR is used in the final output sequence. A 2-to-1 multiplexer is used to make the selection and creates the nonlinear forward transformation

Figure proposed design flow

The objective of a random number generator (RNG) is to produce random binary numbers which are statistically independent, uniformly distributed and unpredictable. RNGs are necessary in many applications like cryptography, communication, VLSI testing, probabilistic algorithms, and so on. RNG randomness evaluation is performed by using a seed encryption

Presented a new LFSR architecture for scan-based BIST that fully exploits the encoding ability of an LFSR by using more than one cells of the LFSR for feeding

the scan chain of the CUT, in different test phases In the proposed technique, the segmentation is performed by simply retaining one copy of a pattern as a reference

pattern and “used to specify whether the successive patterns are Equal or unequal to the retained reference pattern or not.

Test sequences generated by the Geffe generator have large cycle period, and are able to achieve considerably more transitions that those created by linear machines .Geffe generators have equal ability in detecting stuck-at faults in combinational circuits as linear generators do . In the case of diagnosing stuck-at faults in sequential circuits, the Geffe generator performs much better than the linear machines . Because of these benefits, Geffe has been suggested as a desirable pseudo-random pattern generator in the arena of obtaining a high coverage for delay faults and stuck-at faults for sequential circuits.

Using a new, very effective compression scheme based on LUT access

The utilized technique is specified by taking into account the occurrence frequency of multiple kinds of information

VI. PERFORMANCE ANALYSIS

The Figure given below is shown that there is a considerable reduction in time and area based on the implementation results which have been done by using XILINX. The proposed algorithm significantly reduces area consumption when compared to the existing system.

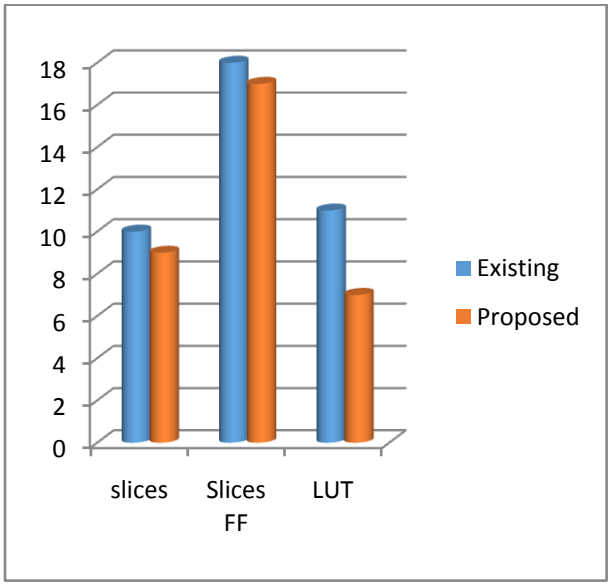

Figure: performance analysis

VI. CONCLUSION

The increasing complexity of modern integrated circuits leads to a critical need for cost-efficient test solutions . To address such test challenges, sophisticated test strategies such as Built-in Self-test (BIST) have been developed over two decades . The fundamental idea in BIST is to integrate the test pattern generation and output response analyzer for the Circuit Under Test (CUT). The redesign by Geffe generator uses the technique of LFSR embedding to reduce the

hardware overhead. According to our experiment, the Geffe modification can cut down area usage on average. More importantly, the fault simulation results show the modified Geffe generator is capable to maintain the fault detection ability of the original Geffe generator. The redesign approach presented in this paper offers a possibility of using Geffe generators in BIST to deliver high fault coverage with reasonable area overhead

REFERENCES

[1] M.Abramovici, M. A. Breuer, and A. D. Friedman, Digital System Testing and Testable Design, IEEE CS Press, New York, 1990.

[2] F.Berglez, D. Bryan, and K. Kozminski, Combinational Profiles of Sequential Benchmark Circuits, Proc. IEEE Int. Symposium on Circuits and System, pp. 1929-1934, 1989.

[3] D.Densmore, "Built-In-Self Test (BIST) implementations an overview of design tradeoffs", Technical paper, University of Michigan, 2001. [Online]Available: http://www.cs.berkeley.edu/~densmore/documents/BIST.pdfI.

[4] P.R.Geffe, "How to protect data with ciphers that are really hard to break", Electronics, Vol 46, pp. 99-101, 1973.

[5] P.Girard, "Survey of low-power testing of VLSI circuits", IEEE Design & Test of Computers, Vol 19, pp. 80 – 90, May-June 2002.

[6] G.Marven, Entropy Based Evaluation of Binary Sequences Produced by ALFSRs, M. Sc. Thesis, Department of Computer Science, University of Victoria, 1994.

[7] M.Puczko and V.N Yarmolik, "Designing cryptographic key generators with low power consumption", Electronic Design, Test and Applications, 2006. DELTA 2006. Third IEEE International Workshop , pp. 418 – 421, January 2006.

[8] J.Zhong and J. C. Muzio, "A comparison of generators for testing sequential circuits using BIST", IEEE International Workshop on Logic & Synthesis, pp. 231-235, May 2003.

[9] J.Zhong and J. C. Muzio, "An investigation of non-linear machines as PRPGs in BIST", International Conference on VLSI, June 2004.

[10] K.Zeng, C. Yang, D. Wei and T. R. R. Rao, "Pseudoramdombit generators in stream-cipher cryptography", IEEE Computer Society, Vol 24, pp. 8-17, February 1991.