Implementation of Error Detection and Correction Codes using VLSI

K.Kaviya Priya, Mr.M.Palaniappan M.E.,
PG Scholar, *Assistant Professor*
Shanmuganathan Engineering College, Arasampatti

Abstract

Errors that affect memories are a major issue in advanced electroniccircuits. As technology scales, multiple bit errors become more likely. This limitsthe applicability of traditional protection techniques like Matrix code or singleerror correction codes that can correct only one error. Multiple errors tend to affectadjacent bits, and therefore it is interesting to use error correction codes that cancorrect adjacent errors. The issue with these codes is that they require a large areaand delay that limits their use to protect flip-flops in circuits. This project presentsthe implementation and evaluation of the encoder reuse technique algorithm forthe detection and correction of multiple transient faults in volatile memories withlow cost implementation .The logic reusable technique is proposed to minimize the area overhead of extra circuits without disturbing the whole encoding and decoding processesour proposed system has been coded in Verilog HDL andsimulated using Xilinx 12.1

I. INTRODUCTION

A parity is involved in older method of error detection. It processed by adding an extra bit to each character. The bit is obstinate by a number of factors such as the type of parity and the data character has the number of logic-one bits

The another structure in code is alliteration code is that discloses to detect error. The coding doodle to attain error-free communication to reveals bit across channel.In data streame data are divided into data bits in data blocks. Every block is transmitted a scheduled number of times. The errors in the same place leads to more problems so it is not effective as parity.They are simple,then used in the transmission of number stations.Error correction is the revelation of errors and mordenization of the original data as error-free data

Fault tolerance is the property that assist a system to extend contriving properly in event of the failure of one or more faults of its constituents.Hamming code is a process that has a set of ECC that can be used for detect and correct bit errors while in data transmission and storage

II. RELATED WORKS

1) Punctured Difference Set (PDS) code is a process to identify the multiple cell upsets in memories

2)The bits by the same logical word into different physical words which has been used in restrain multiple cell upsets in interleaving technique .
3) Built-in current sensors (BICS) are scheduled for reinforcement on correction single error detection and double error detection for granted fortification against multiple cell upsets.
4) 2-Dimentational matrix codes are prospective to conducive correct multiple cell upsets per word with a low decoding delay in which one word has been divided into multiple rows and columb .

Drawbacks:
1) PDS codes require more area, power, and delay overheads since theencoding and decoding circuits are more complex in these
complicated codes.

2) Interleaving technique may not bepractically used in content-addressablememory (CAM), because of the tight coupling of hardware structures from both cells and comparison circuit structures
3) BICS technique can only correct two errors in a word.
4)2D MC is capable of correcting only two errors in all cases.

In the recent technique names as FUEC–triple adjacent error correction (TAEC), is able to correct an error in a single bit, or an error in two adjacent bits (2-bit burst errors) or a 3-bit burst error, or it can detect a 4-bit burst error. This is possible by adding one more code bit. In this case, for a 16-bit data word, the FUEC–TAEC code needs eight code bits. The parity-check matrix H for this code is presented. As in the case of the FUEC–DAEC, *Ci* are the code bits and *Xi* are the primary data bits. Similarly, from H it is very easy to design the encoder/decoder circuitry.But this technique will be considered as less precision which could not correct the large number of datas.

III. PROPOSED SYSTEM

In this paper, we proposes a new algorithm named asData Segmentation Section Code (DSSC)) based on divide-symbol is proposed to provide enhanced memory reliability.This algorithm for the detection and correction of multiple transient faults in volatile memories with low cost implementation.

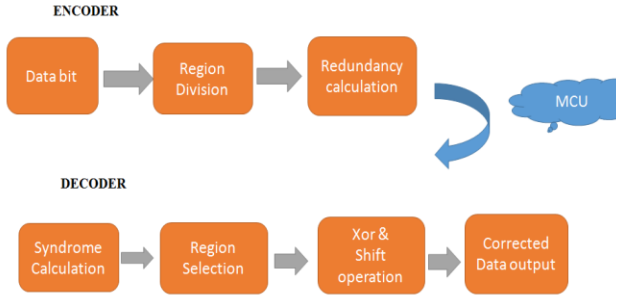

Fig.1 Proposed architecture

Data Segmentation section code is an Error Correction code based on two-dimensional code. The code in this codifies 16 data bits in 32 bits. Thus only parity bits are used for encoding data bits to reduce the area and time conception.

A, Data Segmentation Section Code Encoding Process

Fig.2 shows the structure of 32 bits of data encoded by Data Segmentation Section Code. The cells in gray was data bits,they were divided into four groups (A, B, C, D).

A1	A2	A3	A4	Di1	Di3	CbA13	CbA24
B1	B2	B3	B4	Di2	Di4	CbB13	CbB24
C1	C2	C3	C4	P1	P3	CbC13	CbC24
D1	D2	D3	D4	P2	P4	CbD13	CbD24

Fig.2 DSSC Encoded data model.

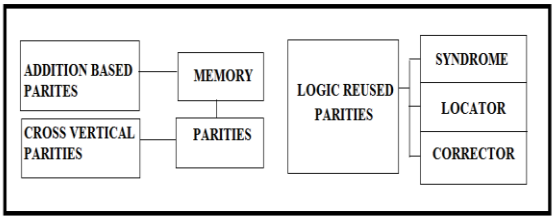

Fig 3 proposed architecture

The cells in green are the *Diagonal bits* (D_i) analyed with XOR operations in specific data bits:

$$Di_1 = A_1 \oplus B_2 \oplus C_1 \oplus D_2$$

$$Di_2 = A_2 \oplus B_1 \oplus C_2 \oplus D_1$$

$$Di_3 = A_3 \oplus B_4 \oplus C_3 \oplus D_4$$

$$Di_4 = A_4 \oplus B_3 \oplus C_4 \oplus D_3$$

The cell in blue was*Parity bits* (P) analyze by XOR operations in the data bits columns:

$$P_1 = A_1 \oplus B_1 \oplus C_1 \oplus D_1$$

$$P_2 = A_2 \oplus B_2 \oplus C_2 \oplus D_2$$

$$P_3 = A_3 \oplus B_3 \oplus C_3 \oplus D_3$$

$$P_4 = A_4 \oplus B_4 \oplus C_4 \oplus D_4$$

The cells orange is a *Check bits* (Cb) analyzed by XOR operations in interleaved bits of each group:

$$CbA_{13} = A_1 \oplus A_3$$

$$CbA_{24} = A_2 \oplus A_4$$

$$CbB_{13} = B_1 \oplus B_3$$

$$CbB_{24} = B_2 \oplus B_4$$

$$CbC_{13} = C_1 \oplus C_3$$

$$CbC_{24} = C_2 \oplus C_4$$

$$CbD_{13} = D_1 \oplus D_3$$

$$CbD_{24} = D_2 \oplus D_4$$

The redundancy bit was analyzed and, the encoding process ends and the 32 bits was stored.The Dibits and Cbbits are arranged between the data bits and Cbbits, in order to develpo the efficiency of Data Segmentation Section Code against Multiple Cell Upsets characterized by adjacent error patterns. Figure describes the mains elements of the parity operation of the Data Segmentation Section Code encoder.

The decoding process of DSSC is divided into three steps:

Syndrome appraisal of the redundancy bits - The syndrome appraisal consists of a XOR operation between the redundancy data stored and the recalculated redundancy bits (RDi, RP, and RCb). So the values for the Syndrome of Diagonal , Parity and Check bits are estimated by:

$$SDi = Di \oplus RDi$$

$$SP = P \oplus RP$$

$$SCb = Cb \oplus RCb$$

Verification of error decoding conditions - After the analysing of the Syndromes, one of these two conditions need to be satisfied before the error correction execution: (i) SDi and SP vectors have at least one value similar to one; (ii) more than one SCb value was similar to one. The conditions permite the algorithm for identify the error for data bits region.

Selection and correcting the wrong data region and correction processes -In this decoding process a distinct region is selected in the data bit and corrected. The region are divided into regions and it is shown below.They split the data bits in three regions and it was elplained so as to select a definitivegroup of bit for the correction process. This reduce the area and the time conception.

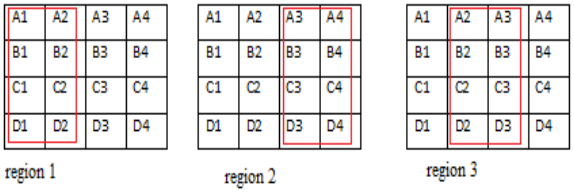

Fig.3 Regions of data bits.

The fig 3(a), (b) and (c) show that region 1, 2 and 3 are formed by data bits distributed in columns (1 and 2), (3 and 4) and (2 and 3), respectively. The selection of which region will be corrected is defined by the integer sum (+) of specific bits of SDiand SP. Table presents a group of equations which describes the criterion for region selection of DSSC, where the region with more syndrome bits equals to 1 is be declared as the wrong one (Region 1 or Region 2). If the sum of the equations presents equal value, then the Region 3 is selected.

Region selected	Criterion to selection
Region 1	$(SDi_1 + SDi_2 + P_1 + P_2) > (SDi_3 + SDi_4 + P_3 + P_4)$
Region 2	$(SDi_1 + SDi_2 + P_1 + P_2) < (SDi_3 + SDi_4 + P_3 + P_4)$
Region 3	$(SDi_1 + SDi_2 + P_1 + P_2) = (SDi_3 + SDi_4 + P_3 + P_4)$

Table1 : Region selection criterion.

For regions 1 and 2, the correction procedure consists in a XOR operation between the region selected and the SCbsmatrix. Region 3 is a special case where it is strictly necessary that neither of all SDi and SP bits are null, even if the condition II of step 2 is satisfied. Note that Region 3 has its first column formed by values with the even index (2), meaning that the correction performed has to be different from the other regions. If region 3 is selected, the correction procedure must be performed by SDi with shifted positions, to align the indexes of SCbs with the matrix of Region 3. In the following section, some correction examples performed by the proposed method are described. Figure summarizes the operation performed by the decoder described in this section.

IV. SIMULATION RESULTS

The proposed circuit are simulated and synthesized by using modelsim and xilinx12.1 which occurs low area than the existing. The experimental results are given in Table2 and the simulation results of layout and the waveforms are shown in the fig.4 and 5. Then the synthesis result of the proposed are shown in fig.6.

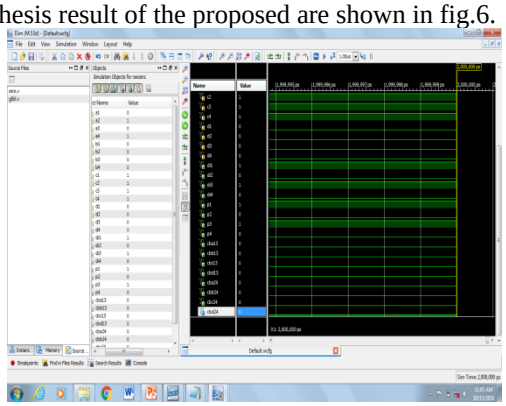

Fig.4 simulation results

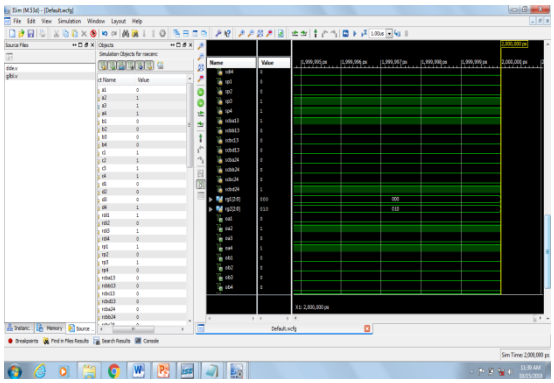

Fig. 5 output waveform of proposed

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Util
Number of Slices	29	960	
Number of 4 input LUTs	50	1920	
Number of bonded IOBs	47	83	

Fig.6 synthesis report of proposed architecture

S.No	Parameter	Existing	Proposed
1	Slice	56	29
2	LUT	96	50
3	IOB	39	47

Table 2: comparison of existing and proposed results

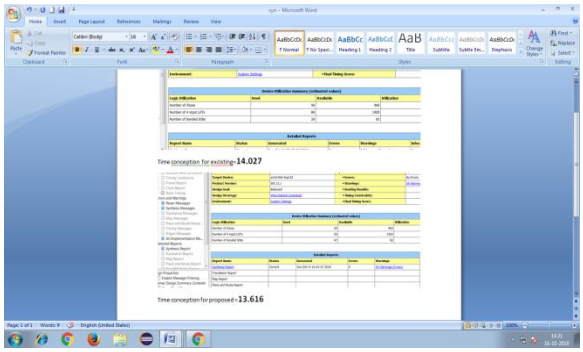

Fig.7:time conception for existing and proposed.

S.No	Time for existing	Time for proposed
1	14.027	13.616

Table 3: Compatision of time

V. PERFORMANCE ANALYSIS

The Figure given below is shown that there is a considerable reduction based on no of transistors and the performance chart has been shown below in fig.7

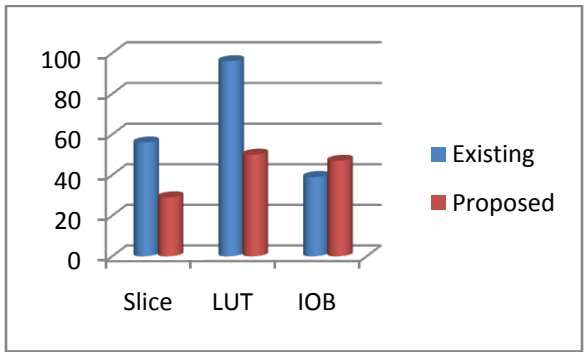

Fig.8 performance analysis

VI. CONCLUSION

This project proposes with Data Segmentation Section Code this is an error detection and correction code to memory devices exposed to MCUs. By using this code on parity code and enclosed to handle with more Multiple Cell Upsets. Data Segmentation Section Code exhibited the lowest cost of coading, low area and improve time conception. Though, hamming and Extended Hamming codes in the ECCs Matrix brought advantages in error coverage it increased heavily the cost of both codes, when compared with Data Segment Section Code.In redard to the exprobated results, Data Segmentation Section Code offering the dominant results for all fault summeries, where that Data Segmentation Section Code has the high performed compromise between error coverage and in lower area and in time conception by the analyse.

REFERENCES

[1] P.Hazucha, C. Svensson. Impact of CMOS technology scaling on the atmospheric neutron soft error rate. IEEE Transaction on Nuclear Science, v. 47, n. 6, pp. 2586-2594, Dec. 2000.

[2] K.LaBel, C. Barnes, C. Marshall, A. Johnston, R. Reed, J. Barth, C. Seidleck, S. Kayali, M. O'Bryan. A roadmap for NASA's radiation effects research in emerging microelectronics and photonics. IEEE Aerospace Conference, v. 5, pp. 535-545, 2000.

[3] P.Ferreyra, C. Marques, R. Ferreyra, J. Gaspar. Failure map functions and accelerated mean time to failure tests: New approaches for improving the reliability estimation in systems exposed to single event upsets. IEEE Transaction on Nuclear Science, v. 52, n. 1, pp. 494- 500, Feb. 2005.

[4] V.Gherman, S. Evain, F. Auzanneau, Y. Bonhomme. Programmable extended SEC-DED codes for memory errors. IEEE VLSI Test Symposium (VTS), pp. 140-145, 2011.

[5] D.Radaelli, H. Puchner, S. Wong, S. Daniel. Investigation of multibit upsets in a 150 nm technology SRAM device. IEEE Transaction on Nuclear Science, v. 52, n. 6, pp. 2433-2437, Dec. 2005.

[6] A.Chugg, M. Moutrie, R. Jones. Broadening of the variance of the number of upsets in a read-cycle by MBUs. IEEE Transactions on Nuclear Science, v. 51, n. 6, pp. 3701-3707, Dec. 2004.

[7] J.Maestro, P. Reviriego. Study of the effects of MBUs on the reliability of a 150 nm SRAM device. ACM/IEEE Design Automation Conference (DAC), pp. 930-935, 2008.

[8] R.Hentschke, F. Marques, F. Lima, L. Carro, A. Susin, R. Reis, Analyzing area and performance penalty of protecting different digital modules with hamming code and triple modular redundancy. Symposium on Integrated Circuits and Systems Design, pp. 95-100, 2002.

[9] C.W Slayman.Cache and memory error detection,correction,andreduction techniques

[10] for terrestrial servers and workstations. IEEE Electron Devices Society, v. 5 ,pp. 397 – 404, Sept. 2005

[11] M.Biberstein ; T. Etzion. Optimal codes for single-error correction, double-adjacent-error detection. IEEE Information Theory Society. v:46,pp: 2188 – 2193,sep 2000.