Design and implementation of low power 1-bit full adder cell using GDI technique

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Abstract— *Power consumption has become major design constraint for integrated circuits(IC's). In the Nanometer technology regime, leakage power has become a major component of total power. Full adder is the basic functional unit of an ALU. The power consumption of a processor is lowered by lowering the power consumption of an ALU, and the power consumption of an ALU can be lowered by lowering the power consumption of Full adder. So the full adder designs with low power characteristics are becoming more popular these days. This proposed work illustrates the design of the low-power less transistor full adder designs using cadence tool and virtuoso platform, the entire simulations have been done on 180nm technology, in virtuoso platform of cadence tool with the supply voltage 1.8V. In this paper adder cells are using different techniques. But GDI technique allows the reducing power consumption, low power delay product and propagation delay.*

Keywords— CMOS, delay, full adder , GDI , low power, power delay product.

I. INTRODUCTION

T he addition is an fundamental arithmetic operation. Which are used in most of the VLSI systems those are microprocessors, digital signal processors and any ALUs. In addition to this there are many other tasks like subtraction, multiplication, division and address calculation and etc. Adder will add the two binary numbers, with this nucleus only others tasks are done. To get overall performance of any system addition is the part of that critical path. Recently, Demand of low power VLSI design systems has increased very high because of fast growing technologies in the mobile communications and also in computation. There is very limited power for mobile systems and battery technologies are not in advance as the microelectronics technology. So designers are facing with the more no of problems like high throughput, high speed, small area of silicon and also the low power usage. So the building a low power and high speed adder cells is the great interest.

Why we need the low power?

The power dissipation will have some limitations, those are two types:

The first type is relates to the cooling considerations of high performance of the systems. The high speed circuit will dissipate the big amount of the energy within very less amount of the time, and to generate a good deal of the heat. And this heat will again need to remove by package, in which the integrated circuit is mounted. The heat removal of system may be become the big limiting factor and if suppose the package will cannot be sufficiently dissipates heat and components which are required is very expensive.

The second drawback of this high power circuits are related to an increase in popularity of an electronic device. Those are like laptops, computers, cellular phones and portable video players all these uses batteries as the power source. This type of devices will provide the limited amount of time for operation, for that they required charging. To extend any battery life it requires low power architecture in the integrated circuits.

II. BASIC FULL ADDER:

Full adder is an combinational circuit and this gives the sum of the 3-bits. This will have three input elements, two output elements. In that two of the inputs are variables named as X, Y. And third is Z, which represents carry from the previous lower significant bit. The two outputs are needed because sum of any three binary numbers are in range from 0 to 3, the binary values 2 or 3 will need two digits. Outputs are two needed those are mentioned by the symbols S & C, where S means sum, C means carry. Output S gives value of least significant bit of the sum and variable C gives output carry.

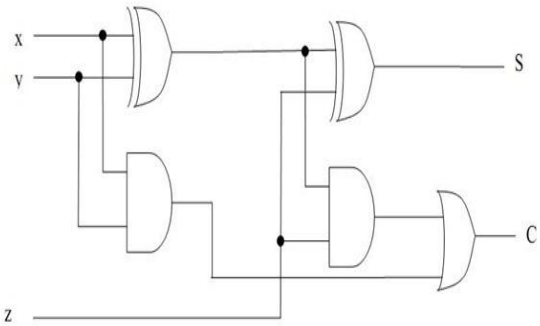

Fig 1: Basic circuit of 1-bit full adder

In the truth table there is mentioned all possible combinations of input variables. With respected to the input variables the outputs sum and carry will get with the expressions of those. And if all the all input variables are equal to 0 then the two outputs are equal to 0. If any one of the input variable is equals to 1 then only the sum output will be equal to 1 and carry output will be 0. If the two input variables are equals to 1 then output of sum equals to 0 and the carry is equal to 1. The special case is that if the input variables of all the three are equal to 1 then the output of sum and the carry is equal to 1. With respect to these operations the equations of the sum and carry is expressed and circuit is implemented with respected logic gates.

Table1: The Truth table of 1-bit basic full adder

X	Y	Z	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The expressions of outputs are

$$S=X'Y'Z+X'YZ'+XY'Z'+XYZ$$

$$C=XY+YZ+XZ$$

This can also implement as two half adders and with one or gate, as mentioned in above figure. The output S is from the second half adder and it is an exclusive-or of z, therefore the output of a second half adder is given by

$$S = z\oplus(x\oplus y)$$

$$S=Z(XY'+X'Y)'+Z'(XY'+X'Y)$$

$$S=Z(XY+X'Y')+Z'(XY'+X'Y)$$

$$S=XYZ+X'Y'Z+XY'Z'+X'YZ'$$

The carry output given as

$$C=Z(XY'+X'Y)+XY$$

$$C=XY'Z+X'YZ+XY$$

A. Different implementation techniques:

Transmission gates, pass transistors and gate diffusion inputs are different techniques in designing of low power digital circuits.

The pass transistors design will have small nodal capacitance which results in very high speed. Amount of transistors used in this is very low so that there is low power dissipation. With the reduced number of transistors occupies small area which leads to the minimized interconnections of the wires. There is mainly two disadvantages of these pass transistor design: one is the threshold voltage across a single channel of the pass transistor, this results to the reduced drive and slow operation. Second one is full swing at output voltage is not possible.

The second technique is transmission gates used to realize the complex logic functions. The degradation voltage level at the output problem can overcome by using this technique. But this technique requires the more area than the pass transistors circuitry and it will requires complemented control signals.

The third technique was gate diffusion technique (GDI), in this the inputs are directly diffused into gates of the transistors are N-type and P-type devices. That's why it is called as gate diffused technique, it reduces power dissipation, area and propagation delay of any digital circuits. This method is based on the simple cell.

B. Advantages of GDI over other technologies:

1. It will have low power system design.
2. It will allow the decreasing of power.
3. The Propagation delay is reduced.
4. Area of the digital circuit will reduces.
5. The Maintaining of low complexity in the logic design.

III. The basic Gate Diffusion input(GDI) Cell

In the last two decades the CMOS technology is resulted so many circuit designs by using different logic styles. Those different topologies are conventional CMOS, pass transistor logic, pseudo NMOS logic and transmission gates. But the work done in all these types of logic styles has given that the output swing of logic CMOS and transmission gate designs are better compared with other logic styles. But the problem is that these logic styles require more number of transistors. Due to this the area will increases, if area increases the usage of power and delay will increases. It means the power and delay will increases if the number of transistors in the circuit is increases. Because of this reason another logic style called GDI (gate diffusion input) was implemented. Using this logic style we can implement larger circuits with less number of transistors, less power and less delay compared with other logic styles. To conclude this statement I have implemented full adder circuit in different logic styles and compared with gate diffusion logic style.

The simple GDI cell will have four terminals they are G (the input for both NMOS & PMOS transistors gates), P (input to the source or drain of the PMOS), and N (input to the source or drain of NMOS).

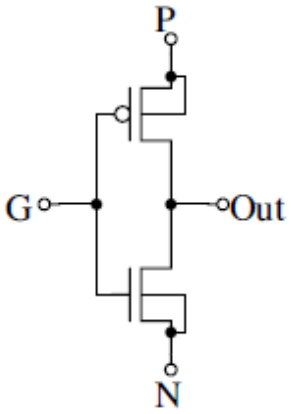

Fig 2: The basic GDI (Gate Diffusion Input) cell

The both bulk terminals of PMOS and NMOS were connected to P & N, so it looks like CMOS inverter and it will be biased at the contrast with an CMOS based inverter.

It will be remarked at all logic functions is not possible in the standard P-Well process, but it will be implement correctly in the Twin-Well CMOS based technologies. The change in input configuration of simple GDI (Gate Diffusion Input) cell is showed below, and it will correspond to the six different Boolean functions.

The below table shows the change in input configuration of GDI cell. Which represents the six different Boolean expressions, but these all expressions are very complex in CMOS. These will uses the 6 to 12 transistors in the standard CMOS implementations. But these are very easy in Gate Diffusion Input method. Why because in this GDI (Gate Diffusion input) technique we are using only 2 transistors to implement all these Boolean functions. This structure is very different from existed CMOS technologies and has some very good features. This will allow the improvements in the design complexity level. The truth table of a simple GDI cell is showed below by implementing some different Boolean functions.

Table 2. Logic functioning of basic GDI cell.

Input at P	Input at G	Input at N	Output Y	Function
B	A	0	A'.B	F1
1	A	B	A'+B	F2
B	A	1	A+B	OR
0	A	B	A.B	AND
B	A	C	A'.B+A.C	MUX
1	A	0	A'	NOT

By using this truth table and design methodology of the GDI cell will gives multiple input gates implementations. The difference between these GDI technology and CMOS technology is based on design. The source of NMOS in GDI structure is not connected to ground and source of PMOS in GDI cell is also not connected to the VDD. So this technique will gives the GDI implementation to an extra two input pins for input use, and which makes GDI cell design to be very flexible than the CMOS design.

In the recent days a structural approach towards the low power adder designs has been improved. In that adder cells are converted into 2 stages. First stage is to generate the intermediate logic functions of the XOR and XNOR. So it's usually developed with the pass transistor logic functions to reduce the transistors count. That's type of complementary outputs all together with respect to their inputs. This will be comes under the second stage. Outputs Sum & Carry is generated from second stage of the full adder.

Based on this technology XOR and XNOR gates are implemented and these are the applications of the GDI technique. Each of these blocks needed four transistors to implement these technologies. But in future its further decreased to three transistor designs and in proposed techniques it will be two transistors only. In the proposed techniques these cells are looks like the MUX cell. Compared with the conventional CMOS techniques this GDI technique will require less number of transistors only. The usage of power is very less and some different features are there which will allow the improvements in the design complexity.

In VLSI design area there are some considerations which are complexity, the static power dissipation, transistors counts and the logic level swing. These all will gives research on GDI because of low power and very high speed. But the GDI method suffers from need of CMOS process, because it requires silicon on insulator or twin-well CMOS process. These are very expensive than standard p-well CMOS process. The former aims to decrease the power consumption and latter to achieve low power delay product by transistor sizing.

IV. The proposed 6 transistor GDI Full Adder

Full adder circuit is implemented with 3 modules. Those modules are 2 XOR or XNOR gates and 1 MUX. To design these modules we have used 2 T based XOR or XNOR gates. To get the sum and carry at the output stages we need these gates. In these 6 transistors there is equal number of PMOS and NMOS transistors. It means to implement 1-bit GDI based full adder we require only 3 PMOS transistors and 3 NMOS transistors. Compared with other implemented logic techniques like CMOS, TGA and PTL it requires very less number of transistors. But the main problem is about threshold voltage loss and noise margin at the output stages. To

avoid this problem we can use buffer at the output stages.

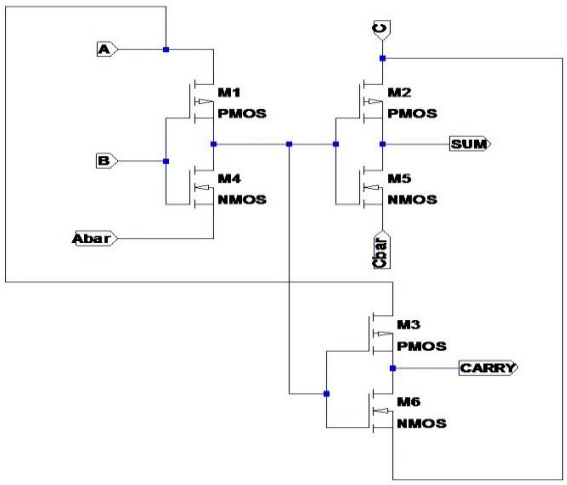

Fig.3: The 6 transistor GDI based Full Adder

V. Simulation and Results

In this section, we want to describe the various adders which are already existed and using in VLSI systems for power consumption and delay and various processers. In this section we are going to discuss about the adders which are 20 transistor transmission gate adder, 10 transistor static energy recovery full adder, 16 transistor transmission function full adder, 10 transistors full adder and 8 transistors full adder. And from the GDI logic we have discussed existed adders like 24T, 10T and also the proposed adders from GDI logic are 8T and 6T. All these adder circuits are implemented in Cadence virtuoso at 180nm technology, respected to these adder circuits we have calculated power, delay and power delay product of these all adder circuits. Compared other logic adders and even from the existed GDI logic our proposed adders consume less power and takes less delay and gives low power delay product.

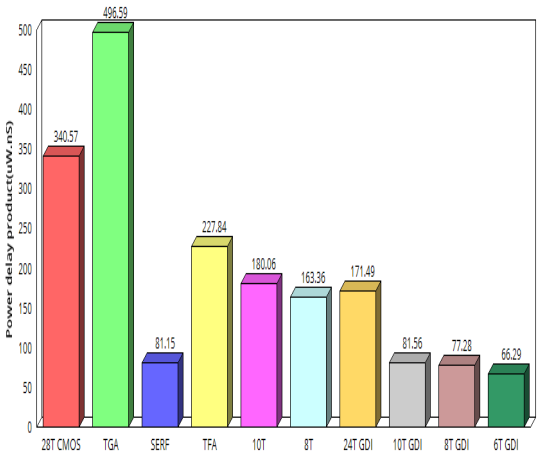

Fig.4 The comparison of Power Delay product (uW.nS) for different full adders

Conclusion

The research process is centered on the "Design and Implementation of a low power 1-bit Full adder cell using GDI technique in Cadence Virtuoso Platform". The main purpose of this thesis is do power reduction and to increase the speed in the 1-bit full adder cell. In this paper GDI technique is introduced and by using this technique we have reduced power consumption, size, and delay. Normally for more transistors to design any full adder, but it requires more area, with that it requires more power and it will gives the more delay. But by using this technique if we use more transistors also the full adder circuit consumes less power and gives the normal delay. With these two parameters the power delay product is decreasing. These all simulations have been done under 180nm technology at 1.8v voltage supply in Cadence Virtuoso Platform.

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