Design of Low Power Single-Ended 12T SRAM Cell and Monitoring NBTI/PBTI

Pavithra V, Geeta R
Assistant professor
Department of Electronics Communication engneering
P.S.R.R college of Engineering for Women
Sivakasi,Tamil nadu, India

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Abstract *- SRAM cells are used in many applications such as VLSI core, micro and multi core processor. SRAM cell improved both read stability and write ability at low supply voltage and power dissipation. This paper presents a robust 12T SRAM using CMOS technology and back to back latch structure of the proposed cell is constructed by two half Schmitt-based inverters, and the proposed cell eliminates the half-selected problem in the write operation using BTI method. Bias temperature instability (BTI) most suitable method to monitoring the input of SRAM cell. In this paper, we proposed method to drive NBTI/PBTI scheme to detect leakage current can be monitored to determine worst case input in the SRAM block. This paper is low area/power overhead in the SRAM cell. This implementation is developed in tanner EDA tool.*

Keywords *- low supply voltage, Bias temperature instability, reliability, SRAM, leakage current.*

I. INTRODUCTION

Power dissipation instead of performance is mainly concerned in the chip design nowadays. Since a major Part of chip power is occupied by SRAM. Low power SRAM is urgently needed. The portable microprocessor controlled devices device embedded memory, which represented a larger portion of the system on chip. these portable systems need ultralow power consumption can be minimized and also recently the demand for low power battery operated device is growth and where needed to low supply voltage, low power SRAM are required to extend system operation time under limited energy resources.

Supply voltage scaling is the most effective way to reduce both switching power and leakage power for CMOS VLSI and designing 12T subthreshold SRAM cell. The method is removes the half-select issue in 6T and 8T SRAM cell and faster read. Since the proposed cell is free from half-select disturb, SRAM cell is better hold noise margin and read performance compared to the Schmitt-trigger based 10T SRAM cell. The half selected cell problem in write operation is eliminated, which makes SRAM cell robust in subthreshold region.

II.RELATED WORK

Ghasem Pasandi and Massoud Pedram (2018) are presented a internal write-back and read-before-write schemes to eliminate the disturbance to the half-selected cell in SRAMs.Internal write-back scheme for single-ended SRAMs and other for differential sensing SRAMs design. This write-back operation to achieve the elimination state of half-selection problems and differential sensing SRAMs operation to improve partial-read operation is needed before the actual write operation compared to half resilient schemes. The proposed design is attractive option for low-power, high performance design. But the problem is distortion in the bits assigning [1].

Chien-cheng yu and ming-chuen shicu (2017) are presented a single port five transistor SRAM cell with improved write-ability and reduced standby leakage current a novel single port 5T sram cell and associated read and write assist is proposed. The proposed design is a two-phase reading mechanism to improve the read speed and avoid unnecessary power consumption. But butter than to 6T and 5T SRAM cell topologies and the design is reduce the half-selected cells disturbance is difficult to the standby leakage in different corner compared with the standard 6T SRAM cell [2].

Vishvakarma S.K and kushwah C.B (2016) are presented a single-ended with dynamic feedback control 8T sub threshold SRAMs cell. Single-ended with dynamic feedback control 8T the design to reduce by differential switch power during read-write operation and to improve the data stability compared to 10T SRAM cell for low leakage and resilient subthreshold design. The proposed cell has higher power saving capability during read and write operation but the problem of design is cannot operated the medium frequency like neural signal processor [3]

III.PROPOSED METHOD

A. The Proposed Sram Cell

The schematic design of 12T SRAM cell is shown in fig1. The cross-coupled structure is formed by back to back latch model and also two half-Schmitt based inverters.

Node PQ and node PQB are the storage nodes, while node Q and QB are true storage nodes. Each of the pseudo nodes is located between the two cascaded NMOS transistors which forms the pull down path of the half-Schmitt based inverter. Their existence is crucial, since they offer an isolation mechanism between bit lines and the true storage nodes during the read operation, and that protects the original storage state. Transistors P1, N1, N2, and N5 constitute the left half-Schmitt based inverter, while transistors P2, N3, N4 and N8 constitute the right half-Schmitt based inverter. Transistors N6, N7, N9 and N10 are write access transistors. Meanwhile, transistors N7 and N10 can also be used in the read path. The read word line (RWL) is row-based, while the write word line (WWL), bit line (BL), and bit line bar (BLB) are column-based.

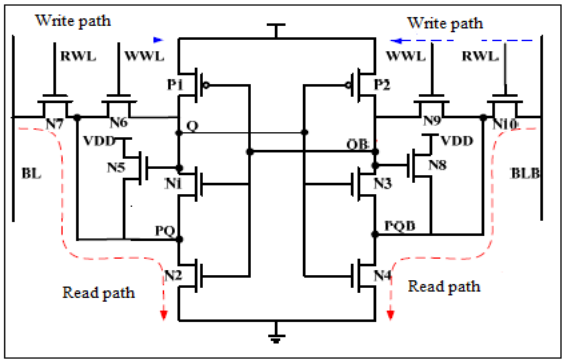

Fig1. The proposed single-end SRAM cell

A.Write Operation And Half-Select Issue

To perform a write operation, RWL and WWL are enabled simultaneously. Hence, the write path in our cell includes two stacked NMOS transistors, as shown in Fig.1, which makes the write performance sacrificed as compared to the 6T and 10T cell. Fortunately, the pseudo node PQ and PQB can also sense the state of the bit lines through transistor N7 and N10, which slightly helps write the data into the true storage nodes to compensate the sacrificed performance.

We employ multiple threshold transistor schemes in our cell to promote the write performance. LVT transistors are applied to transistor N7 and N10, while transistors are applied to the other transistors in our cell. The strong drive ability of transistor can promote the write performance, thus making it almost the same as the 6T and 10T cell. Fortunately, it does not introduce additional peripheral circuit penalty. Most importantly, the employment of transistors N6, N7, N9 and N10 eliminates half-select problem, which remains unsolved for the 6T and 10T cell. Our cell is selected when control signals RWL (row-based) and WWL (column-based) are both active. The half-select cells are in the state that only one of signal RWL and WWL is activated. Consequently, the true nodes Q and QB are isolated from the bit lines in the half-select mode, thus the state of bit lines does not affect the original data.

B. Read operation

To perform a read operation, signal RWL is enabled, whereas signal WWL is disabled. State of each transistor during the read operation, assuming that the data stored at Q is now "1". At this situation, transistors N5 and N4 are activated, which clamps the pseudo node PQ and PQB to the state of "1" and "0", respectively. Meanwhile, transistors N6 and N1 are disabled, thus providing an isolation mechanism between BL and true node Q. Accordingly, the noise in BL does not affect node Q.

Likewise, node QB is isolated from the BLB by transistors N9 and N3. But transistor N3 is enabled in the case and connects the true node QB and pseudo node PQB. Still the noise will not change the original state of QB easily. Since node QB is "0", only high level noise will cause node QB to flip to a wrong state.

Fortunately, there is threshold loss when transistor N3 transfers high level noise. Hence, the noise is suppressed and will not change the state of QB. Meanwhile, node Q is absolutely isolated from the noise and remains at the original state stably, thus the feedback mechanism between node Q and QB also prevents the noise changing the original state of QB.

C. Bti Connected To The Sram Block And Vco

The BTI can be connected to the SRAM block with almost no effect on its normal operation condition. Fig 2 (a) shows this connection. In the test phase, the test signal is triggered high, which turns ON M2. In this case, by writing on the SRAM block, *I*vdd flows into the SRAM block through the vco to measure SRAM cells NBTI aging state. This is while during the normal SRAM block operation, M1 is ON and the WCBS is not in the path of *I*vdd flow.

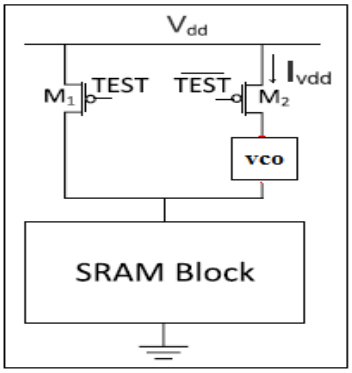

Fig 2(a) Proposed NBTI connection to the SRAM block

As the same way, the connection of VCO to the SRAM blocks, to monitor the maximum of *I*gnd. In

order to measure PBTI aging state, is shown in Fig 2(b) It should be mentioned that the supply voltage of the SRAM block should be separated from the logic block of the SRAM cell, which normally is and *I*vdd/*I*gnd.

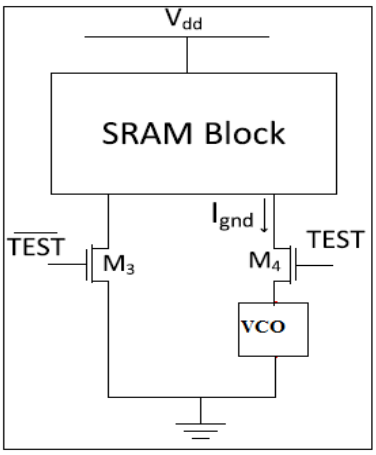

Fig 2(b) Proposed PBTI connection to the SRAM block

During the normal operation of the SRAM block, when the test signal is "0," *M*2 turns OFF and the power of the other parts of the monitor is gated (not shown in the figure for simplicity). The test procedure will be done infrequently within long intervals, which can be once a week or month. Hence, the idle time of the sensing is much more than the working time and the sensor components are usually inactive. Therefore, the BTI effect on the sensing itself is quite negligible. The peak of the overall current, which is drawn from VDD during the write operation, is equal to the total of the write current (dynamic current) and the leakage current of SRAM cells. However, the differences of the peak write current between the fresh and the aged conditions reveal the aging states, not the absolute values of the write current. Hence, the leakage currents existing in two conditions will be eliminated to a large extent and the write current differential variations show the aging states of the SRAM cells.

D. Voltage-Controlled Oscillator

The latched voltage, which is corresponded to the maximum of *I*vdd, is used as the control voltage of the presented VCO with even number of stages of normal inverters and odd number of stages of current starved inverters. One normal inverter is placed after the each current starved inverter; this is because a rail-to rail signal oscillation will be generated by the ring oscillator. This VCO with two normal inverters and one current starved inverter are used in this circuit.

The output frequency of the presented VCO is linearly dependent on the input voltage in the frequency range that a sensor operates. More simulation results are presented in this paper and they determine the current flow of *M*3 and consequently the current flow of *M*1 and *M*4. *M*2 and *M*5 transistors limit the current supply available for the inverter constructed by *M*6 and *M*7; in the other words, the inverter is starved for the current and *M*2 and *M*5 act as current sources. The current in *M*1 and *M*4 is mirrored in each current source stage. Voltage drop at *M*1 and *M*4 turns *M*2 and *M*5 ON and due to equal situations, the current flow of *M*2 and *M*5 is exactly equal to *M*3. This is because *M*1 is always in saturation condition (*V*GD = 0 > *V*th). By assuming that *M*2 is also in saturation condition, the currents of *M*1 and *M*2, called *I*1 and *I*2, according to the saturation current in (1), are linked together with the width to length ratios (*W*/*L*). The relation between *I*1 and *I*2 is given in

$$I_1 = I_2 \left(\frac{W}{L}\right)_1 \Big/ \left(\frac{W}{L}\right)_2$$

Where *(W/L)* 1 and *(W/L)* 2 are the width to length ratio of
*M*1 and *M*2 transistors, respectively. This current is equal
to I3.

IV.SCHEMATIC DIAGRAM OF SINGLE ENDED 12T SRAM CELL

Fig 3.1 shows the schematic design of Single-ended 12T SRAM cell. Design of Single-ended 12T SRAM cell transistor consists of 12T. Fig 3.2 shows the Schematic output Single-ended 12T SRAM cell.

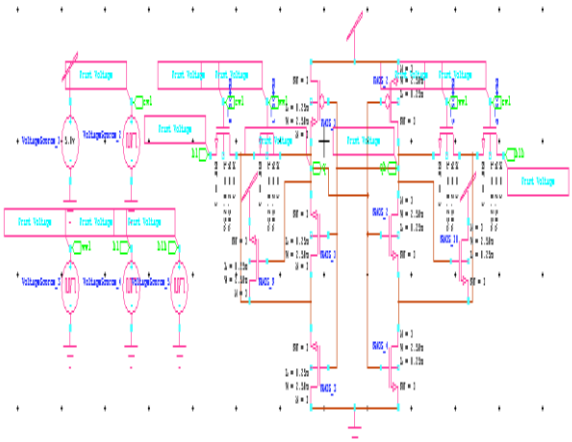

Fig 3.1 Schematic design of Single-ended 12T SRAM cell

V.SIMULATION RESULT OF SINGLE-ENDED DECOUPLED 12T SRAM CELL

The transient response of Single-ended 12T SRAM cell is shown in fig 3.

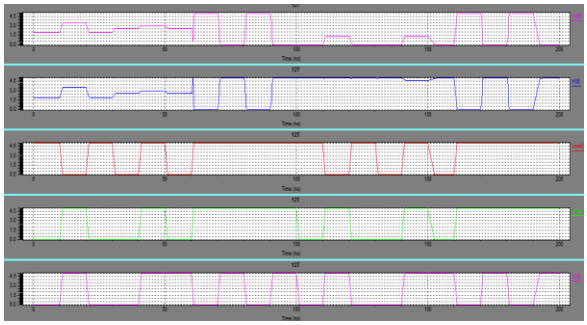

Fig 3.2 Schematic output of Single-end 12T SRAM cell

VI.POWER MEASUREMENT

The power measurement of Single-end 12T SRAM cell. The power consumption of Single-end 12T SRAM cell 1.58147; the power will measure in transient analysis.

VII.ANALYSIS AND COMPARISON TABLE OF SRAM CELL

Table 1 show that the parameter of power consumption is compared with different SRAM cell.

SRAM CELL	POWER(W)
Single-ended with dynamic feedback control 8T sram cell.	2.00765
Schmitt-based 12T SRAM cell	1.58147
NBTI monitoring the 12T SRAM cell	1.60862
PBTI monitoring the 12T SRAM cell	1.58147

Table 1 Performance and comparison of 12T SRAM cell.

VIII.CONCLUSION

A 12T SRAM cell is designed using two half Schmitt-based inverters technique. In this technique is Schmitt-based 12T SRAM cell is read access time faster than compared to 6T convention cell and 10T Schmitt-based SRAM cell and half-selected problem in the write operation is eliminated. The SRAM block is monitor during write operation as an indicator of SRAM cells NBTI/PBTI. The SRAM block is a well-known approach for reducing the SRAM cell leakage current. The new design was compared to existing design using simulation in the 180nm CMOS technology.

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