

Influence of PSSPWM Control analysis on Different Level of Quasi Z Source Cascaded H Bridge Multilevel Inverter

Banupriya M^a, Venkatesan S^{a*}, Indumathi S^a

^a Department of Electrical and Electronics Engineering,

A.C. Govt. College of Engineering and Technology, Karaikudi, Tamilnadu, India.

Abstract—

Multilevel Inverters (MI) has a unique feature which is taking more considerable attention to recent research in power electronic applications. In this work, an integrated inverter topology of quasi z source cascaded H bridge multilevel inverter (QZSCMI) has used to moderate the total harmonic distortion (THD) in the output performance also components. To improve the performance of integrated topology, the phase shift sinusoidal pulse width modulation (PSSPWM) technique has used at different level. The simulation was analyzed and estimated with Fast Fourier Transformation(FTT). As compared to conventional multilevel inverter, the integrated topology has attained significant reduction in output voltage THD value and low electro-magnetic interference.

Keywords: Multilevel Inverter, Quasi Z source cascaded H Bridge, PSSPWM controller.

I. INTRODUCTION

Recently, power electronics converter plays an energetic role in medium and high power applications due to increasing penetration of renewable energy such as solar, wind and demand requirements in terms of efficiency and reliability. Initially, a conventional inverter converts a dc input voltage to a symmetric ac output voltage of desired magnitude and frequency. The output waveform of the inverter should be sinusoidal. However, the output voltage waveform of conventional inverter is non-sinusoidal and contains certain harmonics. To overcome the drawbacks of the conventional inverter multilevel inverter has been introduced.

Multilevel Inverters (MI) inherent features such as improved quality of output waveforms, lower total harmonic distortion (THD), smaller filter size, lower electromagnetic interference (EMI), smaller common-mode (CM) voltage and it can operate with a lower switching frequency are gaining more attention for different applications. Basically, three different types of topologies in multilevel inverter have been presented such as (i) diode clamped multilevel inverter (ii) flying capacitor multilevel inverter (iii) cascaded H-bridge

multilevel inverter. However, some drawbacks are presented in these inverters. In diode clamped multilevel inverter, for more than three levels, the charge balance gets disturbed and Output voltage gets limited. In flying capacitor multilevel inverter Clamping capacitors need to be precharged at a certain voltage and it requires a large number of bulk capacitors. Compared with other topologies, cascaded H-bridge multilevel inverter has some advantages such as it does not require an additional component like diodes and capacitors, more scalable operation Voltage sharing between devices is automatic, allows redundancy by using more number of cells per phase, high voltage can be easily achieved and the circuit is completely modular. Based upon the attractive features cascaded multilevel inverter was implemented in various applications.

In this work, quasi z source inverter also integrated with multilevel inverter to improve the boosting capability. Quasi-Z source based multilevel inverter topology for DC-DC power conversion has attracted a lot of interest due to its advantages of voltage bucking and boosting capability, high gain when compared to the conventional inverter topologies. At first, conventional voltage source inverter (VSI), ac output voltage is limited to less than the dc input voltage. To overcome this disadvantage, a dc-dc boost converter has been additionally added to obtain the required voltage level. Owing to use of this boost converter which is increases the cost and decreases the efficiency of the inverter. To avoid this situation QZSCMI was proposed. In this traditional dc link is replaced by impedance network then the dc voltage is boosted through the shoot through state. Therefore, its number of components was reduced and reliability has been improved. The performance of this inverter is also enhanced by Pulse width modulation techniques. Compared with other PWM techniques phase Shifted Sinusoidal Pulse Width Modulation which was produced the low total harmonic distortion to get a better sinusoidal output waveform.

In this paper presents an integrated inverter topology of quasi z source H-bridge multilevel inverter due to its valuable merits when evaluated with conventional voltage source inverters and Z-

source Inverters. The comparison of five level and seven level Phase Shifted Sinusoidal Pulse Width Modulation controlled QZSMI was performed and evaluated through the simulation. Simulation of single phase QZSCMI for the different level has been carried and estimated using Fast Fourier Transformation analysis in Matlab/Simulink tool.

II. PROPOSED TOPOLOGY

The Quasi Z-Source inverter circuit differs from that of conventional quasi Z Source Inverter in LC impedance network interface between the source and inverter. The Quasi Z Source inverter (QZSI) extends several advantages over Z Source inverter such as continuous input current, reduced components rating, and enhanced reliability. These advantages make the Quasi Z source inverter (QZSI) suitable for power conditioning in renewable energy system. The quasi Z Source Inverter (QZSI), have been derived from the original ZSI Fig.1.

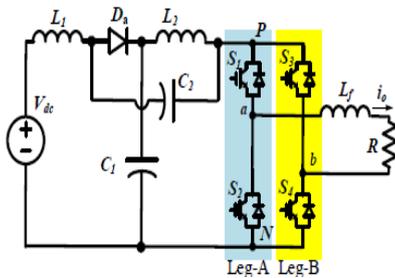


Fig. 1. Basic circuit of quasi Z source inverter

In the same manner as the traditional ZSI, the QZSI has two types of operational states at the dc side: the non shoot through states (the six active states and two conventional zero states of the traditional VSI) and the shoot through state (in the both switches in at least one phase conduct simultaneously). In the non shoot through states, the inverter bridge view from the dc side is equivalent to a current source. The equivalent circuits of the two states are as shown in Fig.2 and Fig.3. The shoot through state is forbidden in the traditional VSI, because it will cause a short circuit of the voltage source and damage the devices. With the QZSI and ZSI, the unique LC and diode network connected to the inverter bridge modify the operation of the circuit, allowing the shoot through state. This network will effectively protect the circuit from damage when the shoot through occurs and by using the shoot though state, the quasi Z-source network boosts the dc-link voltage. The major differences between the ZSI and QZSI are the QZSI draws a continuous constant dc current from the source.

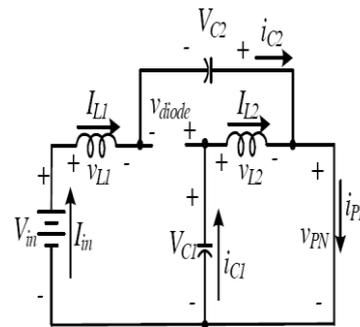


Fig. 2. Equivalent circuit of shoot through state

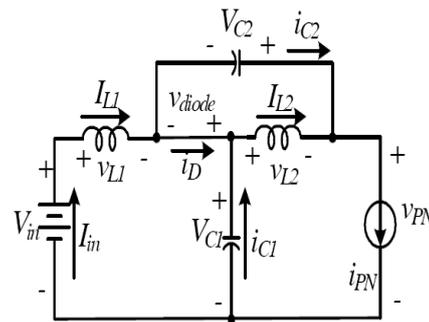


Fig. 3. Equivalent circuit of non shoot through state

All the voltages as well as the currents are defined in and the polarities are shown with arrows. That duration one switching cycle T, the interval of the shoot through state is T₀; the interval of non shoot through states is T₁; thus one has T= T₀+T₁and the shoot through duty ratio, D= T₀/T. Which is a representation of the inverter during the interval of the non shoot through states T₁. The voltage and Average current of the QZSI and ZSI network are shown in Table 1. The stress on the ZSI is shown as well for comparison, where

- (1) M is the modulation index; is the ac peak phase voltage; P is the system power rating.
- (2) $M = T_1 / T_2 - T_0$; $n = T_0 / T_1 - T_0$ thus $m > 1$; $m - n = 1$;
- (3) $B = T / T_1 - T_0$ thus $m + n = B$, $1 < m < B$

From Table 1. We can find that the QZSI inherits all the advantages of the ZSI. It can boost a voltage with a given boost factor. It is able to handle a shoot through state. Therefore it is more reliable than the conventional VSI.

Table 1. Voltage and Average Current of the QZSI and ZSI Network.

	$V_{L1} = V_{L2}$		V_{PN}		V_{diode}	
	T_0	T_1	T_0	T_1	T_0	T_1
ZSI	mV_{in}	$-nV_{in}$	0	BV_{in}	BV_{in}	0
qZSI	mV_{in}	$-nV_{in}$	0	BV_{in}	BV_{in}	0
	V_{C1}		V_{C2}		\hat{V}_{in}	
ZSI	mV_{in}		mV_{in}		$MBV_{in} / 2$	
qZSI	mV_{in}		nV_{in}		$MBV_{in} / 2$	
	$I_{in} = I_{L1} = I_{L2}$		$I_{C1} = I_{C2}$		I_D	
ZSI	P / V_{in}		$I_{PN} - I_{L1}$		$2I_{L1} - I_{PN}$	
qZSI	P / V_{in}		$I_{PN} - I_{L1}$		$2I_{L1} - I_{PN}$	

A. Pulse Width Modulation

The most common and popular technique of sine wave generation is a pulse width modulation (PWM). The PWM technique involves the generation of a digital voltage waveform, for which the duty cycle is modulated such that the voltage of the waveform corresponds to a pure sine wave.

In the most straight forward implementation, generation of the desired output voltage is achieved by comparing the preferred reference waveform (modulating signal) with a high-frequency triangular ‘carrier’ wave as depicted. Depending on whether the signal voltage is larger or smaller than the carrier waveform, either the positive or negative dc bus voltage is applied at the output. Note that all over the period of one triangular wave, the average voltage applied to the load is proportional to the amplitude of the signal (assumed constant) during this period. The resultant chopped square waveform contains a replicated of the desired waveform in its lower frequency components, with the higher frequency components being at frequencies of an close to the carrier frequency. Notice that the RMS value of the ac voltage waveform is still equal to the dc bus voltage, and hence the total harmonic distortion is not affected by the PWM process. The harmonic components are simply shifted into the higher frequency range and are automatically filtered due to inductance in the ac system.

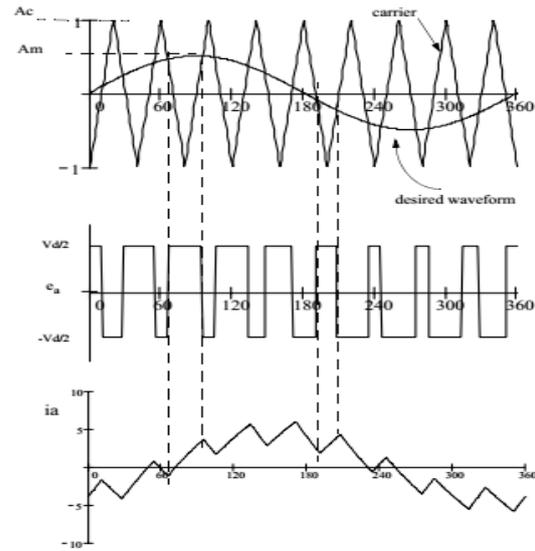


Fig. 4. Principal of Pulse Width Modulation

B. Sinusoidal Pulse Width Modulation (Spwm)

The Sinusoidal Pulse Width Modulation (SPWM) technique is one of the most popular PWM techniques which is suitable for harmonic reduction of the power converters. Sinusoidal Pulse Width Modulation is widely used in power electronics to get output waveform by using sequence of voltage pulses which can be generated by the on and off of the power switches in the converter.

SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. The width of these pulses are modulated to obtain inverter output voltage control and to reduce its harmonic content.

- reference signal (modulating or control signal) - sinusoidal in the case we are going to learn
- carrier signal (triangular wave that controls the switching frequency)

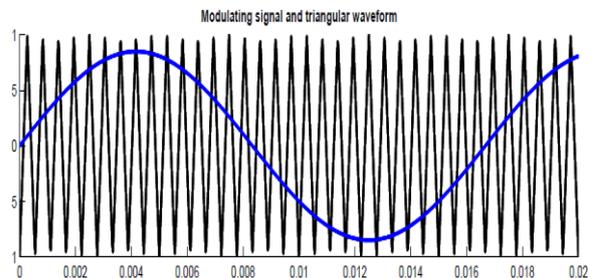


Fig. 5. Sinusoidal Pulse width modulation

C. Phase Shifted Sinusoidal Pulse Width Modulation

In this paper phase shifted based sinusoidal pulse width modulation techniques is presented and shown in Fig. 6. The reference voltage is continuously compared with each of the phase shifted carrier signals. Each cell is modulated independently using the PWM, which provides an even power distribution among the cells. A phase shifted of $180^\circ/m$ for the cascaded multilevel inverter is introduced across the cells to generate a stepped multilevel output voltage waveform with lower harmonic distortion, where ‘m’ is the number of full bridge inverter in a multilevel phase leg. For n-level converter, (n-1) phase shifted signals are generated. The carriers between the inverters are phase shifted $180^\circ/m$. If the reference is greater than the carrier signal, then the active device corresponding to that carrier is switched off.

By using this, carrier signals are shifted and compared with a sinusoidal signal to determine the generated output voltage of the converter due to attractive features of low THD, high equivalent switching frequency and equal distributions of power and semiconductor stress.

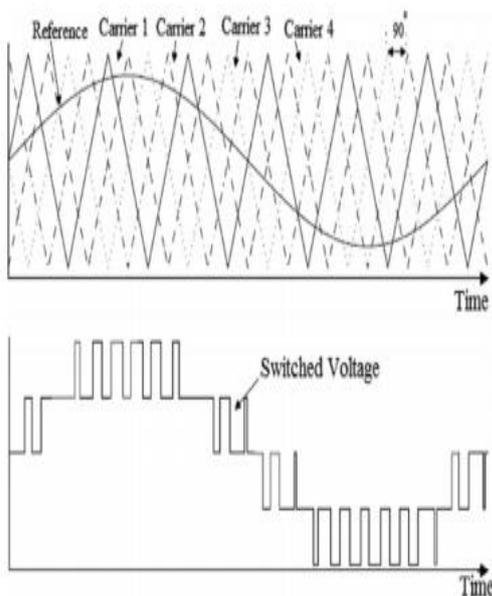


Fig. 6. PSSPWM with switched phase voltage

III. PROPOSED SYSTEM

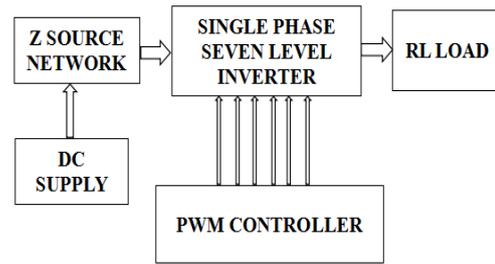


Fig. 7. Block diagram of proposed system

The proposed system integrates a cascaded single phase quasi Z-source and h bridge multilevel inverter topologies. When the dc supply is given to this topology, it was boost the voltage and produce the sinusoidal output waveform which has a low harmonic distortion. In addition, using phase shift sinusoidal pulse width modulation the value of total harmonic distortion has reduced to low value and performance of this inverter was increased.

CIRCUIT DIAGRAM

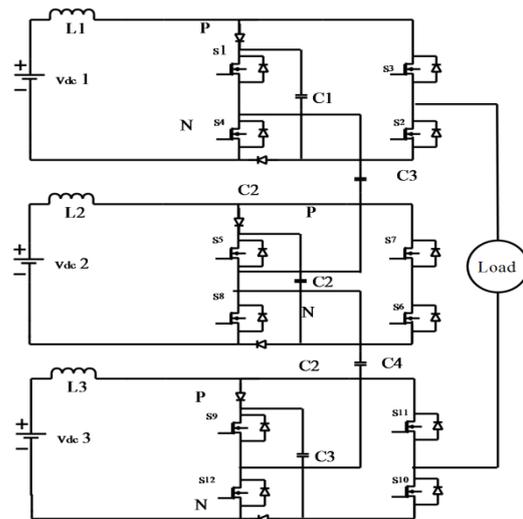


Fig. 8. Proposed QCHBSLBI

The configuration of the proposed single phase quasi cascaded H-Bridge seven level boost inverter is Fig. 8. The proposed inverter consists of three separate DC source, three quasi boost inverter module and capacitor filter connected in resistive load in series. Each module contains five capacitor, three boost inverter, twelve switches, and six diode. The output voltage of proposed QZSCMI has seven levels.

Table 2. Switching scheme for seven level CMI

S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₁ '	S ₂ '	S ₃ '	S ₄ '	S ₅	S ₆	V _{ab}
1	0	0	1	1	0	0	1	1	0	0	1	+3 V _{dc}
1	0	0	1	1	0	0	1	1	0	1	0	+2 V _{dc}
1	0	0	1	0	1	0	1	1	0	1	0	+1 V _{dc}
1	0	1	0	0	1	0	1	1	0	1	0	0
0	1	1	0	0	1	1	0	1	0	0	1	-1 V _{dc}
0	1	1	0	0	1	1	0	0	1	0	1	-2 V _{dc}
0	1	1	0	0	1	1	0	0	1	1	0	-3 V _{dc}

The quasi Z source inverter boost the dc-link voltage. Comparing with the normal quasi Z source inverter, the impedance are arranged so as to form the represented structure of QZSI. The proposed Quasi Z source inverter based seven level cascaded multilevel inverter is controlled with their AC outputs transiting between the seven distinct voltages. They are: +3V_{dc}, +2V_{dc}, +V_{dc}, 0, -V_{dc}, -2V_{dc}, -3V_{dc}. To obtain the seven levels inverter, the required switching scheme is given in Table. 2. The presented QZSI is expected to performed better, since performance limitations commonly associated with dead-time delay which was avoided. The QZSI is responsible for the voltage boost up inverter. The inversion is performed by a supplying PWM signals to the switches of the circuit in a certain fashion so as to produce seven levels at the output. QZSI is a symmetrical network. The operating states of the QZSI are shoot through zero state and non-shoot through zero state. In this proposed inverter the number of bridges required is 3 hence it consists of 12 switches.

IV. SIMULATION AND RESULTS

A. Five Level QCHBMLI

First, five level inverter topology was simulated to confirm the properties of the under balanced DC source condition. A single phase cascaded H-Bridge multilevel inverters operating principle, performance were tested using MATLAB/SIMULINK. The Table. 4. shows the THD value of the output voltage between the CHBQZSI and the proposed QCHBFLBI. The same parameters as the proposed inverter were used to simulate the conventional CHBQZSI. we can observed that the total harmonics distortion(THD) of output voltage of the proposed inverter is lower than that of CHBQZSI.

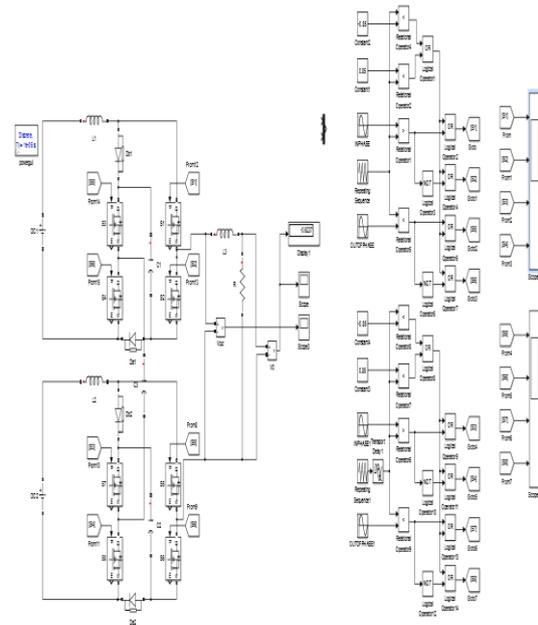


Fig. 9. simulation model of the existing system

The Fig. 10. shows the five level output voltage waveform of the existing system.

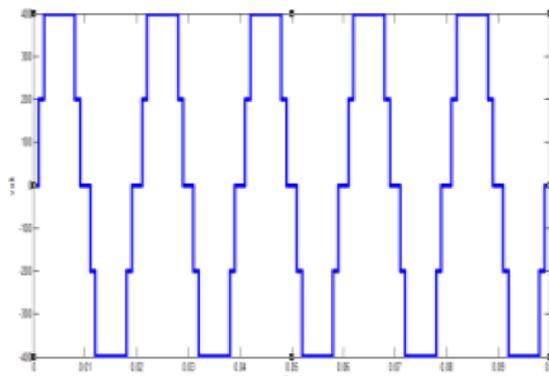


Fig. 10. Existing system five level output voltage waveform

The Fig. 11. shows the FFT analysis of the existing system which has the Total Harmonics Distortion 18.82% .

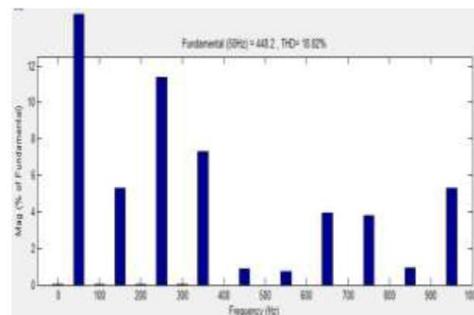


Fig. 11. FFT analysis of existing system

B. Seven Level QZSCMI

The simulation result of the proposed system and the corresponding voltage wave forms are obtained and shown in Fig. 12. and 13.

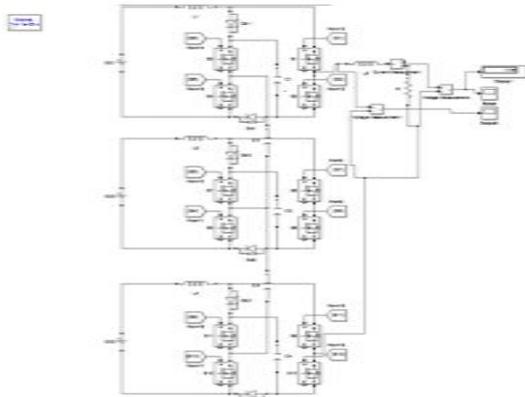


Fig. 12. Simulation model of proposed system

Phase shifted sinusoidal pulse width modulation Generation



Fig. 13. PS-SPWM generation

SIMULATION PARAMETERS

Table 3. provides a list of the simulation parameters for the proposed QZSCMI.

Parameters		Values
Inverter Input voltage		50Vrms
Output Voltage		150V
Output frequency		50Hz
Capacitor		4.4e-3 F
Load	Inductor	3e-3 H
	Resistor	40 Ohms
Switching Frequency		10kHz

The seven level output voltage waveform of the proposed system with amplitude 150V.

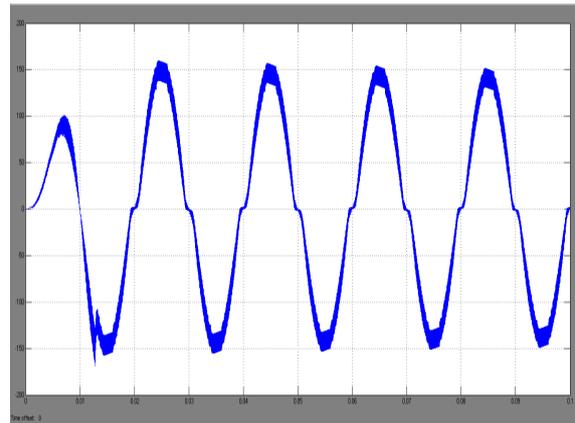


Fig. 14. Seven level output voltage waveform

In this paper the comparison of THD for single Phase cascaded H-bridge multilevel inverter is done in 5 level and 7- level were done using the FFT analysis in MATLAB/SIMULINK. The Total Harmonics Distortion of proposed system is 9.44% which is lower value compare with the existing system.

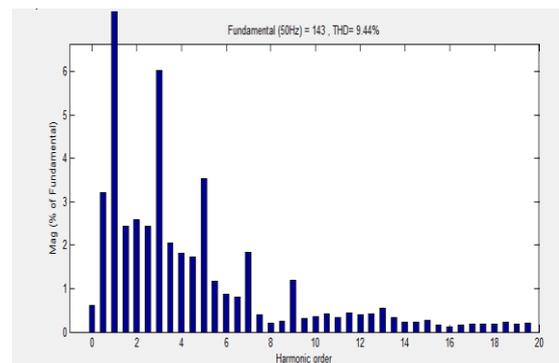


Fig. 15. THD result of proposed system

Table 4. THD Comparison between Existing System and Proposed System

S.no	No .of levels	THD
1	5	18.82
2	7	09.44

V. CONCLUSION

In this paper, the performance of Quasi Z-Source cascaded H-bridge multilevel inverter (QZSCMI) has been investigated based on its THD value. The comparison between single-phase QZSC multilevel inverter with conventional z source inverter was estimated through the FFT analysis. A simulation was carried through Matlab/Simulink for five and seven level of QZSC multilevel inverter with RL load. Input voltage across each the inverter was maintained at 50V and the obtained output 400V. In

QZSC multilevel inverter, PSSPWM control technique has used to reduce the THD value. It has obtained 9.44% of THD value which is lower than the conventional inverter. Due to lower THD value, the output distortion has reduced and better output waveform has been obtained.

REFERENCES

- [1] M.Tawhidha, A.Rijuvana Begum, S,Balakrishnan,Smitha Elsa Peter,A.Sujatha Priyadharshini,K.Vinoth."Design and simulation of seven level cascaded H-Bridge quasi z source multilevel inverter for solar pv system",IEEE Trans ind.Power electron., vol.2,no.5,Nov to Dec 2015.
- [2] B.Ge,Y.Liu,H.Abu-Rub,R.S.Balog,F.Z.Peng,S.McConnell,and X.Li,"Current ripple damping control to minimize impedance network for single phase quasi z source system",IEEE Trans.Ind.Informat.,vol.12,no.3,PP.1054-4848,june 2016
- [3] Balachandra Pattanaik,S.Murugan,"Cascaded H-Bridge seven level inverter using carrier phase shifted PWM with reduced DC sources.IEEE power electrons.,vol.9,no.3,2017.
- [4] J.Napoles,A.J.Watson,J.J.Padilla,J.I.Leon,L.G.Franqualeo, P.W.Wheeler,and M.A. Aguirre,"Selective harmonic mitigation technique for cascaded H-bridge converters with nonequal DC link voltages,"IEEE Trans.Ind.Electrons.,vol.60,n0.5,pp.1963-1971,may 2013
- [5] E.Villanueva,P.Corra,J.Rodriguez and M.Pacas,"Control of a single phase cascaded h-bridge multilevel nverter for grid connected photovoltaic syste,"IEEE Trans.Ind electrons. Vol.56,no.11,pp.4399-4406,Nov 2009.
- [6] [Yushan Liu, Haitham Abu Rub,"An effective control method for quasi z source cascaded multilevel inverter three phase grid tie photovoltaic power system",IEEE Trans ind electron,2014
- [7] Pablo Lezana,Jose Rodriguez,"Cascaded multilevel inverter with regeneration capability and reduced number of switches",IEEE Trans ind electron.,vol.55,No.3,Mar 2008
- [8] D.Sun,B.Ge,F.Z.Peng,A.Haitham,D.Bi,Y.liu,"A new grid connected pv system based on cascaded h bridge quasi z source inverter,"in 2012 IEEE Trans ind.Electron.,no.,pp.951-956,28-31 May2012
- [9] Z.Du,L.M.Tolbert,J.N.chiasson,and B.Ozpineci,"Reduced switching frequency active harmoic elimination for multilevel converter,"IEEE Trans ind Electron.,vol.55,no.4,pp.1761-1770,Apr.2008
- [10] M.K.Nguyen,Y.C.Lima and S.J.park,"A Comparison between single phase quasi z source and quasi switched boost inverter,"IEEE Trans Ind Electron.,vol.62,no.10,pp.6336-6344,Oct.2015
- [11] S.Kouro,M.Malinowski,K.Gopakumar,J.Pou,L.G.Franquel, B.Wu,J.Rodriguez,M.A.Perez,and J.I.Leon,"Recent advances and industrial applications of multilevel converter,"IEEE Trans Ind Electron.,vol. 57,no.8,pp.2553-2580,Aug 2010
- [12] K.H.Law,and M.S.A.Dahidah,"DC-DC boost converter based MSHE-PWM cascaded multilevel inverter control for STATCOM system,"in Proc.IEEE.IPE.,2014,p.1283-1290.
- [13] Y.Yu,G.Konstantinou.B.Hredzak,and V.G.Agelidis,"Operation of cascaded H-bridge multilevel converters for large scale photovoltaic power plants under bridge failures,"IEEE.Trans.Ind.Electron.,vol.62,no.11,pp.7228-7236,Nov.2015
- [14] M.Coppola,F.D.Napoli,P.Guerriero,D.Iannuzzi,S.Daliento and A.D.Pizzo,"An FPGA based advanced control strategy if a grid tied PV CHB inverter,"IEEE Trans.Power Electron,vol.31,no.1,pp.806-816,Jan.2016
- [15] M.Aleenejad,R.Ahmadi,"Fault tolerant multilevel cascaded h bridge inverter using impedance sourced network,"IET Power Electron.,vol.9,no.11,pp.2186-2195,2016
- [16] C.Liu,P.Sun,J.Lai.Y.Ji,M.Wang,C.Chen,and G.Cai,"Cascaded dual boost/buck active frond end converter for intelligent universal transformer,"IEEE Trans Ind Electron.,vol.59,no.12,pp.4671-4680,Dec.2012