Design and Implementation of 16-bit Adder using Carry Select and Carry Save Mode

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Abstract — *Most important digital component in IC design is adders. In almost all computations, addition is used as the most basic operation. Therefore, the design and implementation of binary adders is important considering their area, cost and power. A ripple carry adder has compact area but speed is compromised. A look ahead carry adder is more efficient in terms of computation time but its area is more. Carry select adder is a perfect balance between the two. In this work, a carry select adder has been implemented which does the calculation two times, first assuming the carry to be one and the next one assuming the carry to be zero. It provides a good compromise over cost and time and thereby showing a proper trade-off between time and area complexities. Also, a carry save adder has been analyzed and the design is shown.*

Keywords *— Adder, carry generation, carry propagation*

I. INTRODUCTION

Addition is the most important operation in almost every computational unit say for instance, in microprocessors, digital signal processing, digital image processing etc., also it is the basic operation which is the base for many other complex operations. Area and power are the two crucial factors which are to be concerned in order to increase the portability and better life of portable devices. Even in Personal Computers (PC) and servers, power dissipation is an important design concern. In recent time, most of the computational devices are in thrust of getting area and cost efficient systems and it serves as the most important research area in many domains. The carry propagation serves as the crucial factor in deciding the speed of addition, the faster it propagates the faster is the computation and vice versa. Depending on delay, area and power consumption requirements, several adder implementations have been proposed. Ripple carry adder is the slowest adder as compared to other adders as it works on the principle of rippling the carry which takes time.

Carry select adder (CSL) improves the performance and it is faster and therefore used in many high speed arithmetic calculations and processing applications. By gate level modification of CSL architecture, we can reduce area and power.

The basic motivation of this work is to develop an efficient less area and low power adder. It is clear from Fig 1(a) that the structure has a wide scope of improvement as far as area and power are concerned.

II. CARRY SELECT ADDER (CSL)

The main advantage of CSL [1] is to improve the delay in carry propagation. One way of doing this is to have simultaneously more than one pair of ripple carry adder, in which the carry bit ripples from one stage to next stage. The adder output i.e. sum and the carry out from any stage cannot be produced, until sometime after the carry–in of the stage occurs. This is due to the propagation delay in logic circuitry, which leads to a time delay in the addition process. Therefore, the efficiency of ripple carry adder has been dependent on the delay in carry propagation from previous stage to next stage. The CSL has been popularly used to improves the performance of arithmetic unit by independently generating the multiple carries and then selecting the required carry output to give the final output.

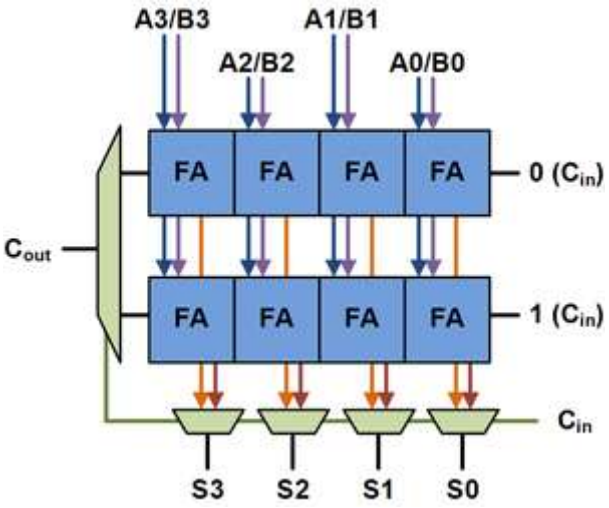

Fig. 1 (a) Basic block of CSL adder

Fig. 1(a) shows the basic block sketch of 4 block CSL adder. As shown in the figure, two adders are multiplexed and resulting carry and sum bits are selected by the carry-in [11]. Here, one ripple carry adder works with the assumption of carry-in to be 0 and the other one with the assumption of carry-in to be 1, the desired result can be obtained by selecting the correct assumption.

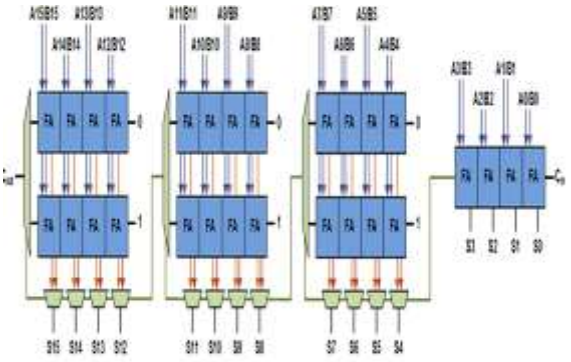

Fig. 1 (b) Basic block diagram of Carry select adder

Fig. 1(b) represents a basic block sketch of CSL adder. A 16-bit CS adder with a periodic block size of 4 can be created with three of these blocks and a 4-bit ripple carry adder [11]. We can make a note of the absence of carry select block in the initial stage of addition, since the initial carry is known to be zero. The time taken by the inputs to reach the output of CSL adder will be cumulative delays of 4 full adder, plus delays of 3 multiplexers.

III. CARRY SAVE ADDER (CS)

Fig. 1(c) shows the basic building block of carry save adder. Carry save adder reduces the implementation of addition of 3 numbers by addition of 2 numbers. CS unit comprises of n full adders and every full adder produces a sum and a carry out for the respective input bit. The final sum can be obtained by shifting the carry sequence left by one place and padding a 0 at the MSB of the intermediate sequence and adding this sequence to the ripple carry adder (RCA) which in turn gives the resulting n+1 value [12].

Continuing this process indefinitely and adding an input or each stage of full adder results in no carry propagation at the intermediate stage. Further, arranging of these staging in a binary tree form with taking into account the cumulative delay logarithmic with respect to the number of inputs also considering the number of bits per input [12]. CS is mainly used in multipliers for efficient CMOS implementation and for high speed digital signal processing applications.

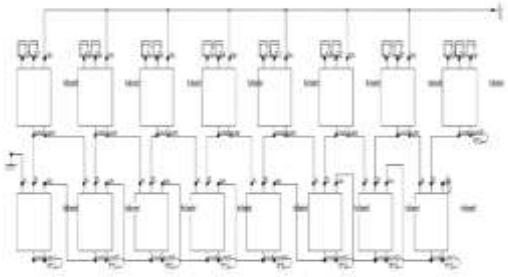

Fig. 1 (c) Basic building block of Carry save adder

IV. DESIGN IMPLEMENTATION

Carry select adder efforts by forming propagate and generate signals (P and G) which depends on whether a carry is being propagated through least significant bit for one of the two inputs being '1' or a carry being created in that position when both the inputs are '1' or a carry being killed in a particular bit position when both the inputs are '0' [2] [13].

Generally P and G are considered to be the two outputs (sum and the carry) of the half adder respectively [2]. In CS adder the carry propagator is propagated to next bit which make this as fast adder. The design steps of 16-bit look ahead carry adder using cadence tool has many steps. First a 4-Bit adder is designed which is elongated to 16-bit adder.

Expressions for 4-bit:
Carry Generation (G) =AB
Carry propagation (P) =XOR (A,B)

Carry(C): C0=G0+P0 CIN
C1=G1+P1 C0
C2=G2+P2 C1
C3=G3+P3 C2
SUM(S):
S0=XOR(A0,B0,C0)
S1=XOR(A1,B1,C1)
S2=XOR(A2,B2,C2)
S3=XOR(A3,B3,C3)

Here, 16-bit carry select adder has been simulated and RTL and technology schematic is generated using Xilinx ISIM 9 simulator in verilog. Fig. 2 represents the block diagram of 16 bit carry select adder.

V. RESULTS

The design shown in this work has been developed using Virtuoso Encounter using typical libraries of TSMC 45 nm or gpdk45. The design constraints and the netlist generated after synthesis are imported to encounter (micro wind) and then from standard cells and routing and placement automated layout can be generated.

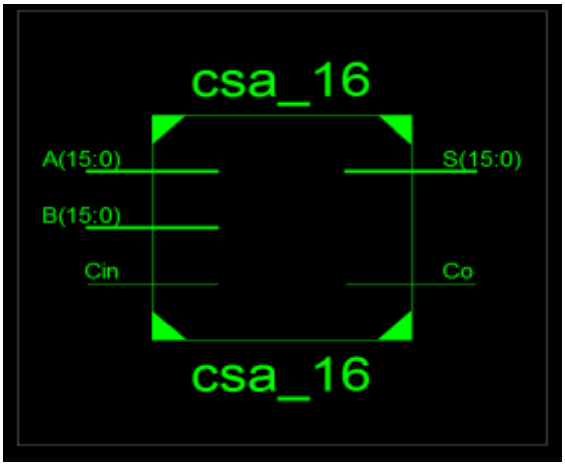

Fig. 2 Block diagram of CSL Adder

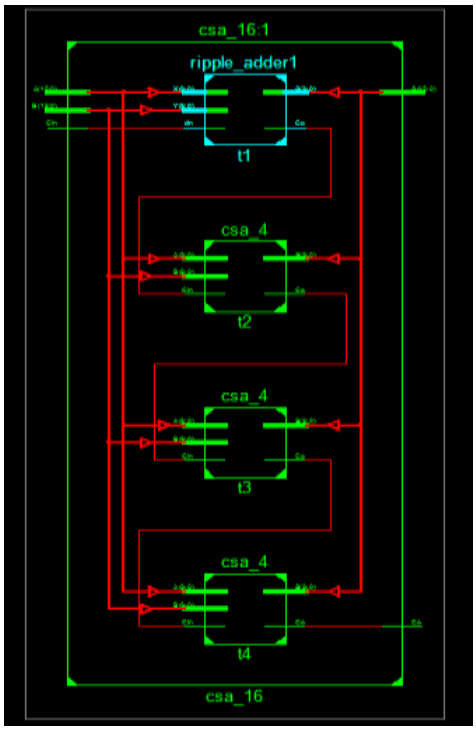

Fig. 3(a) RTL schematic of CSL Adder

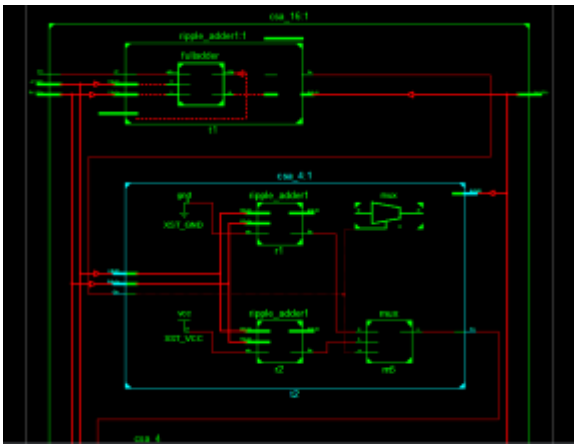

Fig. 3(b) RTL schematic of CSL Adder

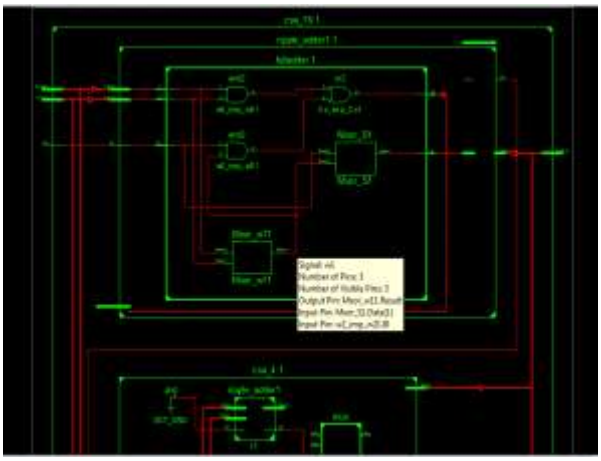

Fig. 4(a) Technology schematic of Carry select Adder

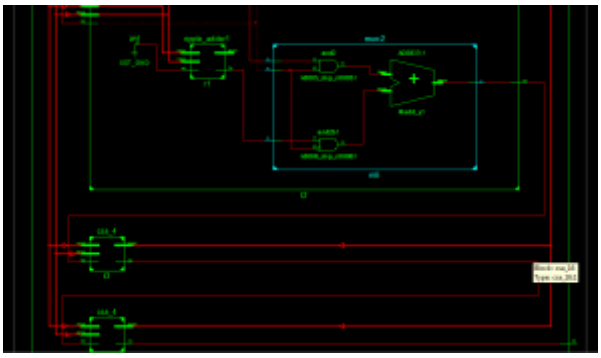

Fig. 4 (b) Technology schematic of CSL Adder

Fig 3 (a) and 3(b) depicts RTL schematic of C adder using cadence virtuoso tool and Fig. 4(a) and Fig. 4(b) depicts technology schematic of CSL adder.

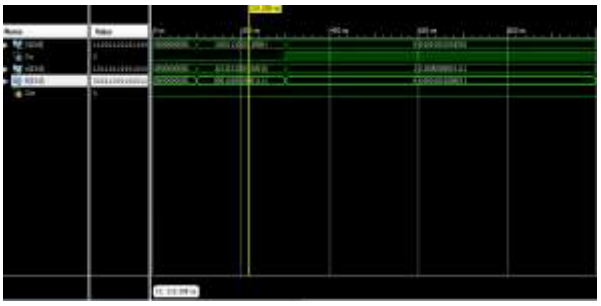

Fig. 5 Simulation result of CSL Adder

Fig. 6 CSL Adder implemented in Virtuoso Encounter

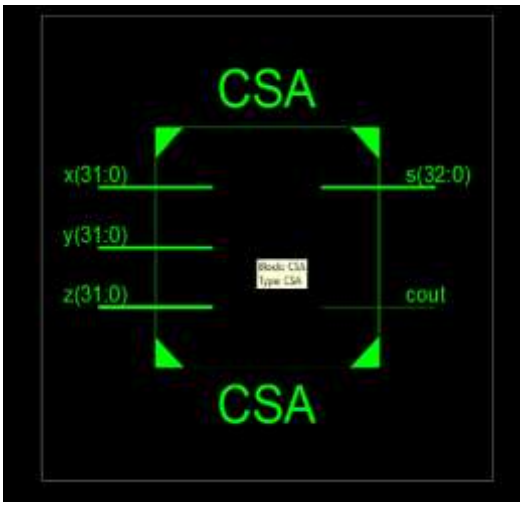

Fig. 7 Block diagram of CS Adder

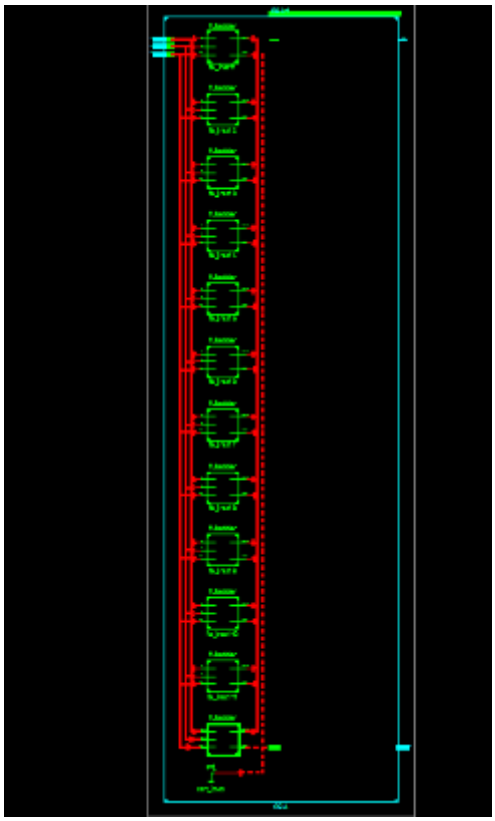
Fig. 8 RTL schematic of CS Adder

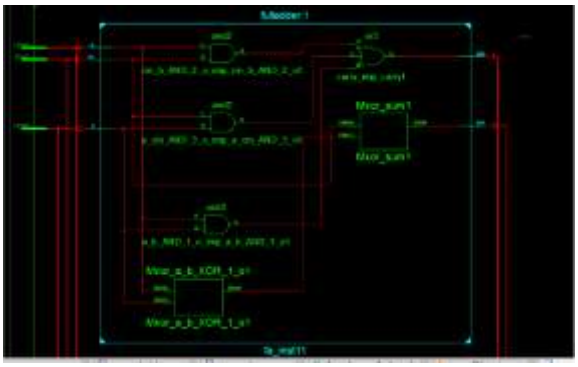
Fig. 9 Technology schematic of CS Adder

Fig 5 shows the simulation output of carry select adder. Fig. 6 shows CSL adder implemented in Virtuoso Encounter. Fig. 7 depicts the block sketch of CS adder. Fig. 8 & 9 depicts RTL and Technology schematic of CS adder.

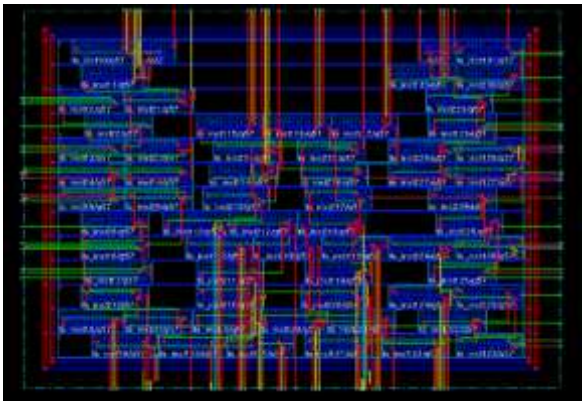
Fig. 10 CS Adder implemented in Virtuoso Encounter

The simulation result has been shown from Fig 2 to 10 and exhibit the regular CSL with respect to area, power and delay. The area shows the total number of MOSFETs in terms of cell area.

The total power includes total internal power, total switching power and total leakage power for sequential, combinational, input-output and clock.

The timing analysis indicates the delay in the arrival of input and output data.

Table 1 Parameter values for CSLA and CSA

Parameter	Value (CSL)	Value (CS)
Total internal Power	77.7596%	70.617%
Total Switching Power	22.1350%	29.2819%
Total Leakage Power	0.1054%	0.1034%
Input Delay	2us	2us
Begin point arrival time	2us	2us
XOR Gate delay	2.095us	2.01 us
OR Gate delay	0.069 us	0.069us
Full Adder delay	0.088 us	0.088 us
Clock Delay	0.084 us	0.84 us

VI. CONCLUSION

Our idea has been successfully implemented in this paper and the results clearly show that the performance has been improved with respect to area and power consumption using CSL and CS architecture as shown in the figure that the number of gates has been reduced. The results show that the CSL architecture is simple and efficient and can be used for compact and highly efficient applications for VLSI design [14].

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