Design of single-ended and differential Ring oscillators in submicron dimensions

Aravinda Koithyar, Sanjeev Sharma

Department of ECE, New Horizon College of Engineering, Bengaluru, India
aravindak@newhorizonindia.edu, hod_ece@newhorizonindia.edu

Abstract *— In this article, the design and simulation results of single ended as well as differential ring oscillators are presented. The empirical equations are made use of, for the purpose of design and comparison. For the single ended ring oscillator, initially a 5-stage circuit is utilized, with different Beta ratios. Later on, the circuit simulation is performed from 5-stage till 23-stage, and the output is obtained as 3.0817 GHz and 0.6705 GHz respectively. Similarly, for the differential ring oscillator, initially a 7-stage circuit is utilized, with different Beta ratios. Later on, the circuit is simulated from 3-stage till 21-stage, and the output is obtained as 2.6925 GHz and 0.3756 GHz respectively. The difference in between the computed and the simulated output with single ended and differential ring oscillators is found to be 3.64% and 1.98% respectively.*

Keywords *— Single ended ring oscillator, Differential ring oscillator, Delay cell, Stage delay, Beta ratio***.**

I. INTRODUCTION

For oscillators in any electronic system, there are two design choices in the range of GHz – either LC oscillator or Ring oscillator. LC oscillators work on resonance of tuned circuit whereas Ring oscillators work on the charging and discharging of the parasitic capacitances of the MOS devices. The LC oscillators have better noise performance, whereas they provide lesser tuning range, and they require larger area, due to the spiral inductors [1]-[3]. On the other hand, the Ring oscillators occupy lesser area and provide wider tuning range.

With Ring oscillators, there are two design choices – singled ended and differential. The Single Ended Ring Oscillator (SERO) is constructed using CMOS inverters, and has the advantages of lesser power consumption, lesser size, ease of design, and larger signal swing. The Differential Ring Oscillator (DRO) is constructed using delay cells, and has better noise performance, larger tuning range and better speed-power product [4]. The SERO can have only odd number of stages, whereas the DRO has the flexibility of using both even and odd number of stages, with the design changes in the delay cell [5].

Fig. 1 shows the circuit diagram of the SERO, in which the inverters are implemented using CMOS design. Fig. 2 shows the block diagram of the DRO, and Fig. 3 shows the circuit diagram of the conventional delay cell for the DRO. The outputs of the delay cell are connected as inputs to the delay cell of the next stage, as shown in Fig. 2.

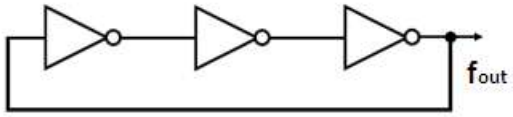

Fig. 1. Gate level diagram of 3-stage Ring oscillator

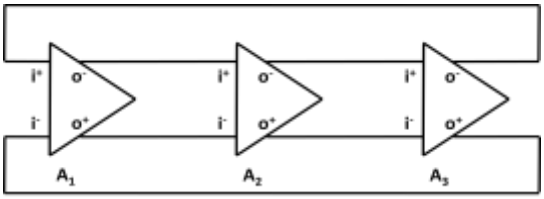

Fig. 2. Block diagram of a 3-stage DRO

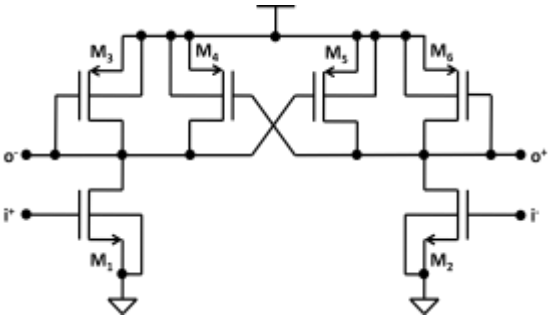

Fig. 3. Circuit diagram of conventional delay cell for DRO

The period of the operating frequency of both of these oscillators is based on the propagation delay of each stage. This delay has to pass through the stages twice, for the completion of one cycle. Hence, utilizing the no. of stages (N) and the stage delay (t_d),

the frequency of operation is conventionally expressed as –

$$f_{osc} = \frac{1}{2\,N\,t_d} \quad (1)$$

Even though the ring oscillator is based on digital logic, it has no stable logic states, and thus, one cycle of oscillation consists of two transitions [6]. Therefore, the frequency of operation can also be expressed as,

$$f_{osc} = \frac{1}{N\,(t_{pLH}+t_{pHL})} \quad (2)$$

II. RELATED PREVIOUS WORKS

For obtaining the propagation delay, different approaches are followed in the literature. In case of SERO, the gate capacitance of the inverter is utilized, and delay is computed in terms of the effective capacitance and the switching current [7], [8]. This is expressed in (3).

$$t_d = \frac{C_{total}V_{dd}}{I_D} \quad (3)$$

The Miller capacitance effect is included (3), and hence, this expression is quite useful for the designer [9], [10]. But, with reference to the switching transition, this expression yields the total capacitance, $C_{tot}=2.5(C_{OXp}+C_{OXn})$. The designer needs to perform the current calculations [11], [12]. In addition, this particular modeling is primarily meant for the micrometer dimensions, and thus, the submicron parasitic effects are ignored. Therefore, the modeling and usage of (2) is advantageous, when compared to that of (3).

In case of DRO, the conventional delay cell is characterized in terms of its stage delay [13], [14]. The expression for the output frequency is in terms of the supply voltage and the drain current. Thus, the designer has to compute the drain currents of all the devices. This is partially performed in [15]. Another expression for the output frequency is obtained by means of load resistance and load capacitance at the output node of the delay cell [16]. But as the load values remain uncomputed, the work remains incomplete.

Instead of these approaches, if a direct expression is available for the designer for a given technology, then the design and simulation efforts are reduced to a large extent. An effort has been made in that direction, in which, the expression for the output frequency is obtained using the switching model of the transistors, with the inclusion of all parasitic capacitances for the submicron behavior [17], [18]. The derived expression is empirically corrected, after comparing the same with the simulated results. In this particular work, the derived expressions for both types of ring oscillators are utilized for the purpose of design and comparison, and the results are evaluated accordingly.

III. CIRCUIT SIMULATION OF SERO

The CMOS implementation of SERO is shown in Fig. 4. A weak p-MOSFET is used as keeper, in order to reduce the start-up time of the oscillator. As the keeper transistor is weak, it is not going to affect the time-period of the oscillator. The output waveform is shown in Fig. 5.

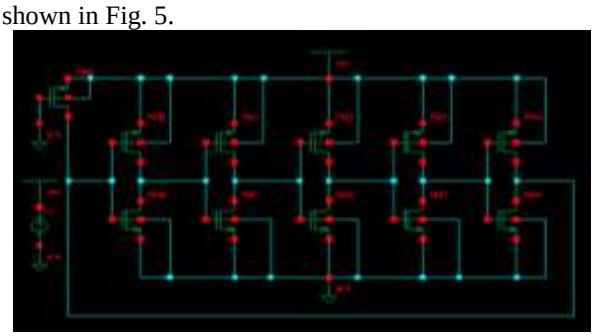

Fig. 4. Schematic diagram of SERO with keeper

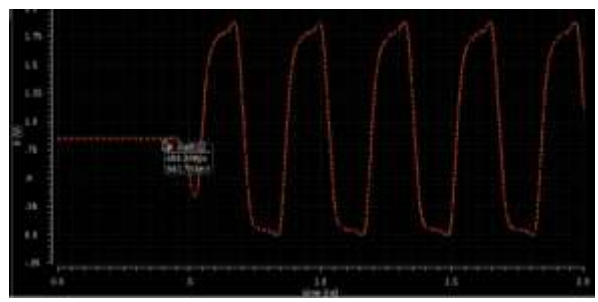

Fig. 5. Output waveform of SERO with keeper

In the circuit, when all P-devices have the same width, and when all N-devices also have the same width, W_p/W_n is called as Beta ratio, provided the channel length for all of them remains the same [19]. This Beta ratio is indicated as "B". In TSMC 180 nm process, the electron mobility is 2.3 times larger than the hole mobility [20]. Therefore, for the purpose of slew balancing, W_p has to be 2.3 times more than W_n. Hence when B = 2.3, for the N-stage SERO, the expression for the frequency of oscillations obtained in [18] is reproduced here as,

$$f_{osc} = \frac{1}{1929.52\,N\,L^2} \quad (4)$$

This equation is utilized for comparing the simulated output frequency value with the computed value. The width of N-MOSFET is chosen from 0.8 µm till 2.4 µm, with the Beta ratio chosen as 1, 2, 2.3 and 3, so as to have a width independent approach. The circuit simulations are performed in two steps - i) with 4 different values of B, for 5 different widths of N-

MOSFET, ii) with 10 different values of N, starting from 5 till 23. The results are tabulated in Tables I & II respectively. From Table I, it can be seen that, when the widths of N and P devices are equal, the deviation is on the negative side, which indicates that such combination is not permissible. For the other Beta ratios, a slight difference is observed, and this is due to ignoring the overlapping capacitance during the derivation of (4).

TABLE I

W_n (µm)	Frequency Values with Variation in B (N=5)			
	B	f_{osc} (GHz) (computed)	f_{osc} (GHz) (simulated)	Deviation %
0.80	1.0	3.1941	3.2776	-2.61
0.80	2.0	3.2775	3.1979	2.43
0.80	2.3	3.1991	3.1240	2.35
0.80	3.0	2.9768	2.9360	1.37
1.20	1.0	3.1941	3.2541	-1.88
1.20	2.0	3.2775	3.1746	3.14
1.20	2.3	3.1991	3.1008	3.07
1.20	3.0	2.9768	2.9129	2.15
1.60	1.0	3.1941	3.2404	-1.45
1.60	2.0	3.2775	3.1646	3.44
1.60	2.3	3.1991	3.0902	3.40
1.60	3.0	2.9768	2.8918	2.86
2.00	1.0	3.1941	3.2300	-1.12
2.00	2.0	3.2775	3.1576	3.66
2.00	2.3	3.1991	3.0817	3.67
2.00	3.0	2.9768	2.8852	3.08
2.40	1.0	3.1941	3.2185	-0.76
2.40	2.0	3.2775	3.1526	3.81
2.40	2.3	3.1991	3.0722	3.97
2.40	3.0	2.9768	2.8835	3.13

TABLE II

N	Frequency Values with Variation in N (W_n=2 µm & B=2.3)		
	f_{osc} (GHz) (computed)	f_{osc} (GHz) (simulated)	Deviation %
05	3.1991	3.0817	3.67
07	2.2851	2.1993	3.76
09	1.7773	1.7123	3.66
11	1.4541	1.4008	3.67
13	1.2304	1.1861	3.60
15	1.0664	1.0274	3.65
17	0.9409	0.9071	3.59
19	0.8419	0.8114	3.62
21	0.7617	0.7341	3.62
23	0.6955	0.6705	3.60

The results that are in Tables I and II are plotted in Fig. 6 and 7 respectively, with Beta ratio being normalized. It is seen from Table II that, for the value of N from 5 till 23, the difference remains almost the same. With this observation, a correction factor which corresponds to the average 3.64% difference, is introduced into (4), so as to obtain an accurate value. Therefore, when B=2.3, the final empirical expression for the operating frequency of SERO is,

$$f_{osc} = \frac{1}{2000\, N\, L^2} \qquad (5)$$

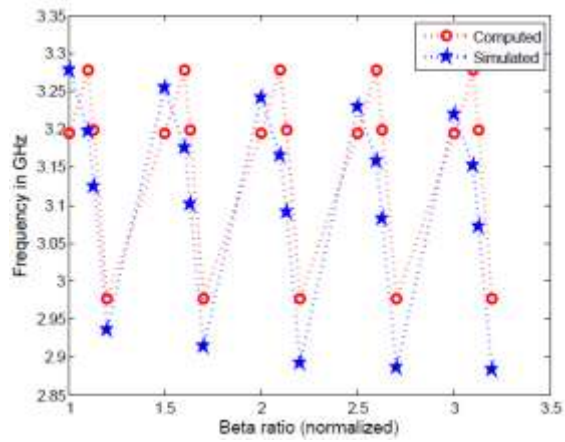

Fig. 6. Beta ratio v/s Frequency of 5-stage SERO

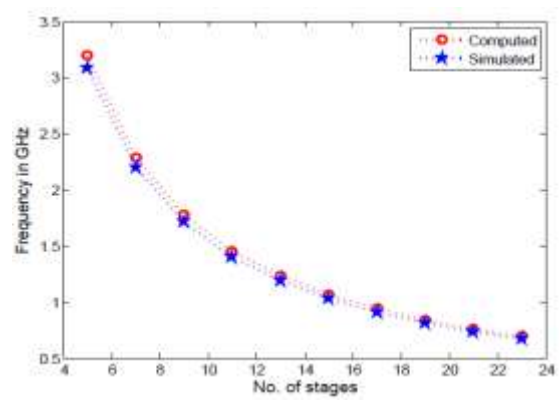

Fig. 7. No. of stages v/s frequency (SERO)

IV. CIRCUIT SIMULATION OF DRO

In a similar fashion, the circuit simulation of DRO is performed. The delay cell shown in Fig. 3 is utilized for each stage, and the block diagram of a 7-stage DRO is shown in Fig. 8, along with its transient analysis in Fig. 9. Following the switching model of the delay cell, the expression for the output frequency is derived as,

$$f_{osc} = \frac{1}{3987.43\ N\ L^2} \qquad (6)$$

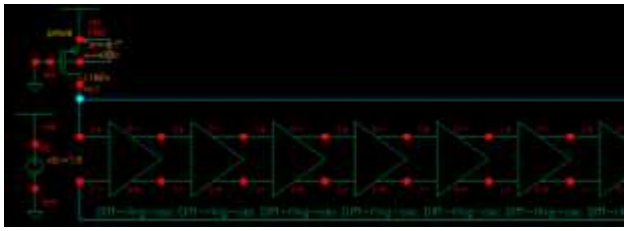

Fig. 8. Circuit diagram of 7-stage DRO

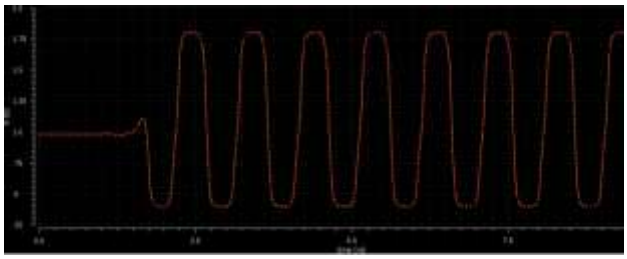

Fig. 9. Transient analysis of 7-stage DRO

As in the case of SERO, the circuit simulation for DRO is also performed in two steps – i) with 5 different values of W_n, and with 4 different values of B, ii) with 10 different values of N, starting from 3 till 21. The results are tabulated in Tables III & IV respectively. The difference in between the simulated and the computed values in Table IV is almost constant, and this difference is again due to the ignoring of overlapping capacitance, during the analysis.

Results that are listed in Table III and IV are plotted in Fig. 10 and 11 respectively, with Beta ratio being normalized. In Table IV, the average difference is found to be 1.98%, which can be introduced as a correction factor into (6), to obtain an empirical expression. Therefore, when B=2.3, the final expression for the output frequency of the DRO is,

$$f_{osc} = \frac{1}{4065\ N\ L^2} \qquad (7)$$

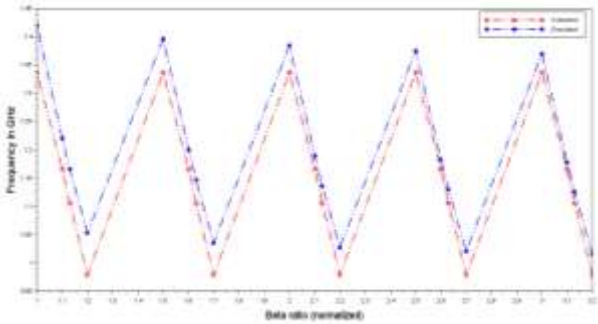

Fig. 10. Beta ratio v/s Frequency of 7-stage DRO

TABLE III

W_n (µm)	Frequency Values with Variation in B (N=7)			
	B	f_{osc} (GHz) (computed)	f_{osc} (GHz) (simulated)	Deviation %
0.80	1.0	1.3369	1.4203	5.87
0.80	2.0	1.1659	1.2197	4.40
0.80	2.3	1.1057	1.1655	5.13
0.80	3.0	0.9788	1.0535	7.09
1.20	1.0	1.3369	1.3968	4.29
1.20	2.0	1.1659	1.2001	2.85
1.20	2.3	1.1057	1.1466	3.57
1.20	3.0	0.9788	1.0348	5.42
1.60	1.0	1.3369	1.3846	3.45
1.60	2.0	1.1659	1.1897	1.99
1.60	2.3	1.1057	1.1359	2.66
1.60	3.0	0.9788	1.0269	4.68
2.00	1.0	1.3369	1.3758	2.83
2.00	2.0	1.1659	1.1825	1.40
2.00	2.3	1.1057	1.1293	2.08
2.00	3.0	0.9788	1.0203	4.06
2.40	1.0	1.3369	1.3703	2.44
2.40	2.0	1.1659	1.1781	1.03
2.40	2.3	1.1057	1.1257	1.77
2.40	3.0	0.9788	1.0149	3.56

TABLE IV

N	Frequency Values with Variation in N ((W_n=2 µm & B=2.3)		
	f_{osc} (GHz) (computed)	f_{osc} (GHz) (simulated)	Deviation %
03	2.5801	2.6925	4.18
05	1.5480	1.5841	2.28
07	1.1057	1.1293	2.08
09	0.8600	0.8784	2.09
11	0.7036	0.7174	1.92
13	0.5954	0.6070	1.91
15	0.5160	0.5261	1.93
17	0.4553	0.4642	1.92
19	0.4073	0.4149	1.82
21	0.3685	0.3756	1.88

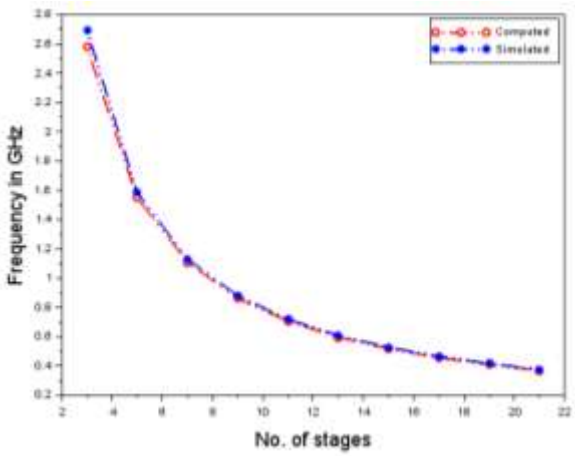

Fig. 11. No. of stages v/s frequency (DRO)

V. CONCLUSION

The CMOS circuits of single ended as well as differential ring oscillators are simulated, and the output frequency values are compared with the computed equations. In both of the cases, it is found that the output frequency is inversely proportional, to the number stages, and to the square of the channel length; the width of the devices has no role. In addition, the following points are observed –

i) With the same number of stages, the single ended ring oscillator produces larger value of frequency than the differential one. This is due to the smaller parasitic capacitance of the inverter, in each stage.

ii) The difference in between the computed and the simulated values is lesser in case of the differential ring oscillator, and this is due to the improved switching performance of the delay cell.

The designer can choose an appropriate type of ring oscillator that suits the application under consideration. The derived formulae help in arriving at a faster implementation.

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