Data Segmented Logic Reusable Error Detection And Correction Code (Dslr) For Memories

N. Muthu Elavarasi M.E student, Mrs. E. M. Umaselvi M.E., Assistant professor/ECE,
Chandy Engineering College, Mullakkadu, Tuticorin - 628005

Abstract

Errors that affect memories are a major issue in advanced electronic circuits. As technology scales, multiple bit errors become more likely. This limits the applicability of traditional protection techniques like Matrix code or single error correction codes that can correct only one error. Multiple errors tend to affect adjacent bits, and therefore it is interesting to use error correction codes that can correct adjacent errors. The issue with these codes is that they require a large area and delay that limits their use to protect flip-flops in circuits. Data segmented logic reusable error detection and correction code.The logic reusable technique is proposed to minimize the area overhead of extra circuits without disturbing the whole encoding and decoding processesour proposed system has been coded in Verilog HDL and simulated using Xilinx 12.1

I. INTRODUCTION

A parity is involved in older method of error detection. It processed by adding an extra bit to each character. The bit is obstinate by a number of factors such as the type of parity and the data character has the number of logic-one bits

Anotherstructure in code is alliteration code is that discloses to detect error. The coding doodle to attain error-free communication to reveals bit across channel. In data stream data are divided into data bits in data blocks. Every block is transmitted a scheduled number of times. The errors in the same place leads to more problems so it is not effective as parity. They are simple, then used in the transmission of number stations.Error correction is the revelation of errors and modernization of the original data as error-free data

Fault tolerance is the property that assist a system to extend contriving properly in event of the failure of one or more faults of its constituents.Hamming code is a process that has a set of ECC that can be used for detect and correct bit errors while in data transmission and storage

II. RELATED WORKS

1) Punctured Difference Set (PDS) code is a process to identify the multiple cell upsets in memories

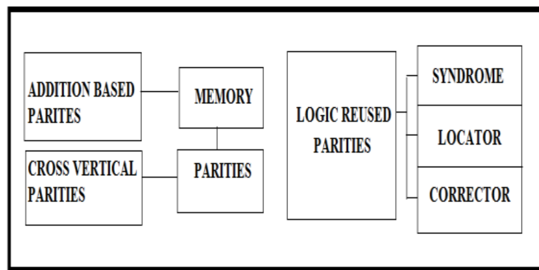
2) The bits by the same logical word into different physical words which has been used in restrain multiple cell upsets in interleaving technique.
3) Built-in current sensors (BICS) are scheduled for reinforcement on correction single error detection and double error detection for granted fortification against multiple cell upsets.
4) 2-Dimentational matrix codes are prospective to conducive correct multiple cell upsets per word with a low decoding delay in which one word has been divided into multiple rows and column .

Drawbacks:
1) PDS codes require more area, power, and delay overheads since theencoding and decoding circuits are more complex in thesecomplicated codes.
2) Interleaving technique may not bepractically used in content-addressablememory (CAM), because of the tight coupling of hardware structures from both cells and comparison circuit structures
3) BICS technique can only correct two errors in a word.
4)2D MC is capable of correcting only two errors in all cases.

In the recent technique names as FUEC–triple adjacent error correction (TAEC), is able to correct an error in a single bit, or an error in two adjacent bits (2-bit burst errors) or a 3-bit burst error, or it can detect a 4-bit burst error. This is possible by adding one more code bit. In this case, for a 16-bit data word, the FUEC–TAEC code needs eight code bits. The parity-check matrix H for this code is presented. As in the case of the FUEC–DAEC, Ci are the code bits and Xi are the primary data bits. Similarly, from H it is very easy to design the encoder/decoder circuitry.But this technique will be considered as less precision which could not correct the large number of data's.

III.PROPOSED SYSTEM

The proposed schematic of fault-tolerant memory is depicted in Fig. 1. First, during the encoding (write) process, information bits D are fed to the DSLR encoder, and then the addition based redundant bits and cross vertical redundant bits are obtained from the DSLR encoder. When the encoding process is completed, the obtained DSLR code word is stored in the memory. If MCUs occur in the memory, these errors can be corrected in the decoding (read) process. Due to the advantage of decimal algorithm, the proposed DSLR has higher fault-tolerant capability with lower performance overheads. In the fault-tolerant memory, the DSLR technique is proposed to reduce the area overhead of extra circuits and will be introduced in the following sections.



A. Proposed DSLR Encoder

In the proposed DSLR, first, the divide-symbol and arrange-matrix ideas are performed, i.e., the N-bit word is divided into k symbols of m bits ($N = k \times m$), and these symbols are arranged in a $k1 \times k2$ 2-D matrix ($k = k1 \times k2$, where the values of $k1$ and $k2$ represent the numbers of rows and columns in the logical matrix respectively). Second, the addition based redundant bits *are* produced by performing decimal integer addition of selected symbols per row. Here, each symbol is regarded as a decimal integer. Third, the cross vertical redundant bits *are* obtained by binary operation among the bits per column. It should be noted that both divide-symbol and arrange-matrix are implemented in logicalinstead of in physical. Therefore, the proposed DSLR does not require changing the physical structure of the memory.

The addition based redundant bits *can* be obtained by addition as follows:

$A4A3A2A1A0 = D3D2D1D0 + D11D10D9D8$

$A9A8A7A6A5 = D7D6D5D4 + D15D14D13D12$

And similarly for the addition basedredundant bits $A14A13A12A11A10$ and $A19A18A17A16A15$, where "+" represents decimal integer addition.

For the cross vertical redundant bits, we have

$V0 = D0 \oplus D16$ (3)

$V1 = D1 \oplus D17$ (4)

And similarly for the rest cross vertical redundant bits. The encoding can be performed by decimal and binary addition operations from (1) to (4). The encoder that computes the redundant bits using multibit adders and XOR gates is shown in Fig. 3. In this figure, $H19 - H0$ are horizontal redundant bits, $V15 - V0$ are cross vertical redundant bits, and the remaining bits $U31 - U0$ are the information bits which are directly copied from $D31$ to $D0$. The enable signal En will be explained in the next section.

B. Proposed DSLR Decoder

To obtain a word being corrected, the decoding process is required. . Second, the addition based syndrome bits $_H4H3H2H1H0$ and the cross vertical syndrome bits $S3 - S0$ can be calculated as follows:

$$\Delta H_4H_3H_2H_1H_0 = H_4H_3H_2H_1H_0' - H_4H_3H_2H_1H_0$$

$$S_0 = V_0' \oplus V_0$$

and similarly for the rest cross vertical syndrome bits, where "−" represents decimal integer subtraction. When $_H4H3H2H1H0$ and $S3 - S0$ are equal to zero, thestored codeword has original information bits in symbol 0 where no errors occur. When $_H4H3H2H1H0$ and $S3 - S0$ are nonzero, the induced errors (the number of errors is 4 in this case) are detected and located in symbol 0, and then these errors can be corrected by

$D0correct$

$= D0 \oplus S0.$ (7)

The proposed DSLR decoder is depicted in Fig. 4, which is made up of the following sub modules, and each executes a specific task in the decoding process: syndrome calculator, error locator, and error corrector. It can be observed from this figure that the redundant bits must be recomputed from the received information bits D and compared to the original set of redundant bits in order to obtain the syndrome bits $_H$ and S. Then error locator uses $_H$ and S to detect and locate which bits some errors occur in. Finally, in the error corrector, these errors can be corrected by inverting the values of error bits.

In the proposed scheme, the circuit area of DSLR is minimized by reusing its encoder. This is called the ERT. The ERT can reduce the area overhead of DSLR without disturbing the whole encoding and decoding processes. From Fig. 4, it can be observed that the DSLR encoder is also reused for obtaining the syndrome bits in DSLR decoder. Therefore, the whole circuit area of DSLR can be minimized as a result of using the existent circuits of encoder. Besides, this figure alsoshows the proposed decoder with an enable

signal *En* for deciding whether the encoder needs to be a part of the decoder. In other words, the *En* signal is used for distinguishing the encoder from the decoder, and it is under the control of the write and read signals in memory. Therefore, in the encoding (write) process, the DSLR encoder is only an encoder to execute the encoding operations. However, in the decoding (read) process, this encoder is employed for computing the syndrome bits in the decoder. These clearly show how the area overhead of extra circuits can be substantially reduced.

IV. SIMULATION RESULTS

The proposed circuit are simulated and synthesized by using modelsim and xilinx12.1 which occurs low area than the existing. The experimental results are given in Table2 and the simulation results of layout and the waveforms are shown in the fig.4 and 5. Then the synthesis result of the proposed are shown in fig.6.

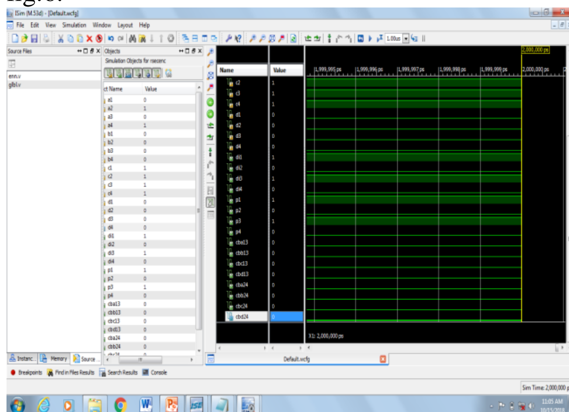


Fig.4 simulation results

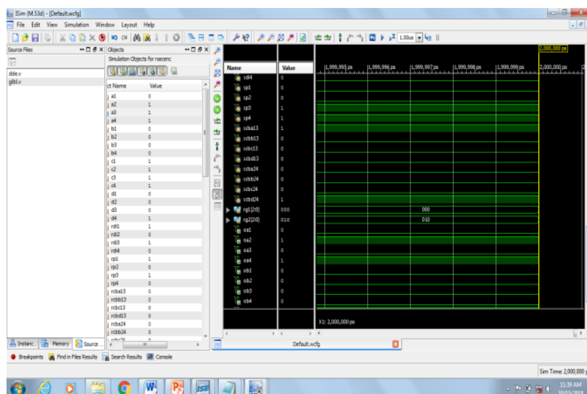
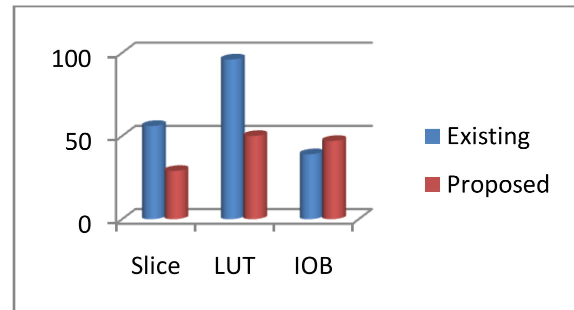


Fig. 5 output waveform of proposed



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Util
Number of Slices	29	960	
Number of 4 input LUTs	50	1920	
Number of bonded IOBs	47	83	

Fig.6 synthesis report of proposed architecture

S.No	Parameter	Existing	Proposed
1	Slice	56	40
2	LUT	96	50
3	IOB	39	68

V. PERFORMANCE ANALYSIS

The Figure given below is shown that there is a considerable reduction based on no of transistors and the performance chart has been shown below in fig.7

100
50
0
Slice LUT IOB
Existing
Proposed

Fig.8 performance analysis

VI. CONCLUSION

This project proposes with Data Segmentation Section Code this is an error detection and correction code to memory devices exposed to MCUs. By using this code on parity code and enclosed to handle with more Multiple Cell Upsets. Data Segmentation Section Code exhibited the lowest cost of coding, low area and improve time conception. Though, hammingand Extended Hammingcodes in the ECCs Matrix brought advantages in error coverage it increased heavily the costof both codes, when compared with Data Segment Section Code. Inregard to the reprobated results, Data Segmentation Section Code offering the dominant results for all fault summaries, where that Data Segmentation Section Code has the high performed compromise between error coverage and in lower area and in time conception by the analyze.

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