Performance Analysis of various adder circuits on 130 nm technology

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Abstract *— A full adder is widely used in application Specific Integrated circuits (ASIC) and also as sub components in chip designs. Different kind of full adder circuitry can be used in various applications to reduce the power dissipation. A low power full adder circuit (20T adder circuits) is designed and its performance is compared is that of a conventional 28T adder. All the circuits are designed using 130nm CMOS technologies & are tested on MENTOR GRAPHICS EDA Tool. Different adders are simulated on basis of speed, power consumption, area and an analysis of delay, power dissipation is carried out with various values of VDD. It is always advantageous to have a low full adder circuit for reducing the overall dissipation of power in design.*

Keywords *— adder, performance, delay, power dissipation, speed & area.*

I. INTRODUCTION

Low power has emerged as a principle theme in today's world of electronics industries. Power dissipation & Delay decides the performance of any component. Single bit addition is a fundamental arithmetic operation performed by full adder. Adders are commonly used in arithmetic circuits like microprocessor, DSP, ALU. All complex arithmetic circuits make use of full adder and hence it is widely used. The overall performance of circuit depends on the delay & dissipated power in the full adder circuit

The design & performance specifications of 28 transmission gate full adder cell is compared with 20 transmission gate adder circuit at 130nm Technology. Different adders on basis of power delay and area were designed and simulated with different supply voltages. Reducing the number of CMOS transistors reduces power consumption.

II. TRUTH TABLE AND EQUATIONS FOR A FULL ADDER

Adding inputs we get sum and carry and the equations to derive the result are given by SUM = X ⊕ Y ⊕ Zin & Carry = XY + YZin + ZinX

Truth Table				
Zin	**X**	**Y**	**C_{OUT}**	**Sum**
0	0	0	0	0
1				1
0		1		
1			1	0
0	1	0	0	1
1				0
0		1	1	
1				1

TABLE 1: TRUTH TABLE FOR FULL ADDER

III. BASIC CONCEPTS

Binary numbers are added using full adder and values carried in & out are taken into consideration. One-bit full adder adds three one-bit numbers. 8, 16, 32, etc. bit binary numbers are added. By cascading adders, Full adders are realised.

It's Custom transistor-level circuit or it can be made of other gates.

A. CMOS LOGIC

Expanded as Complementary Metal Oxide Semiconductor is a technology for constructing ICs. The words "complementary" refers to actually the fact that the design style uses p-type and n-type Metal Oxide Semiconductor Field effect Transistors (MOSFETs) for logic functions.

High noise immunity & low static power consumption are the 2 important characteristics of CMOS devices. This is achieved by having one transistor of the pair always off, significant power is drawn in series combination but momentarily when the on and off states are switched. Due to which, more waste heat is not produced in CMOS devices as compared to other forms of logic.

B. POWER: SWITCHING AND LEAKAGE

When compared to NMOS type of logic circuits , CMOS type of logic dissipates less power. It's because CMOS dissipates power only during switching ("dynamic power"). Dissipation of power is almost zero when it's idle & hence, static CMOS gates are good & power efficient. Many factors such as speed & area had dominated design parameters when compared to power consumption of CMOS logic devices & was not a major concern when designing chips. There is increased power consumption levels as CMOS technology started moving below the sub-micron levels, with respect to per unit area of the chip.

C. BICMOS

Bipolar & CMOS technology are two separate semiconductor technologies that are integrated. It's an evolved semiconductor technology in a single IC

device. High speed, high gain & low output resistance are observed. On the other hand, high input resistance is seen in CMOS technology. It is excellent for constructing simple, low power logic gates. BICMOS technology found application in amplifiers, analog power management circuits and in digital circuits.

D. PASS TRANSISTOR LOGIC

Redundant transistors can be eliminated and it reduces the transistor count to design different logic gates. Instead of directly connecting to supply voltages, transistors are used as switches to pass logic levels between nodes of a circuit.

Designs require low power, runs faster using fewer transistors than designs using CMOS logic.

IV. DESIGN

A. CMOS BASED FULL ADDER CELL

This design mainly consists of both PMOS & NMOS transistors. The transistors in CMOS are arranged in a way that VDD is connected to source of PMOS and ground to source of NMOS. The output is taken at drain terminals & has a full swing. The network is a pull up network.

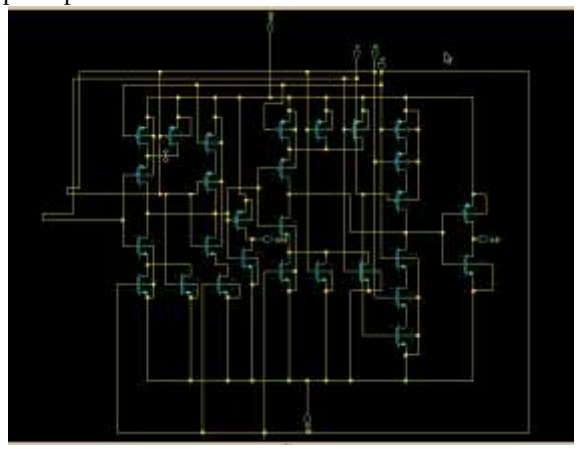

Figure 1: Schematic of Full Adder using 28 T

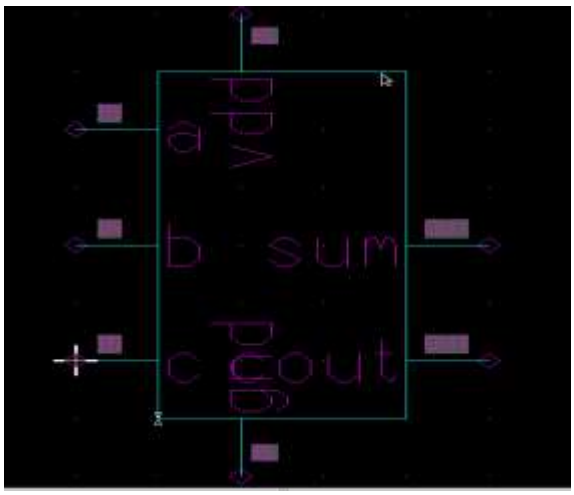

Figure 2 : Symbol For 28 T Full Adder

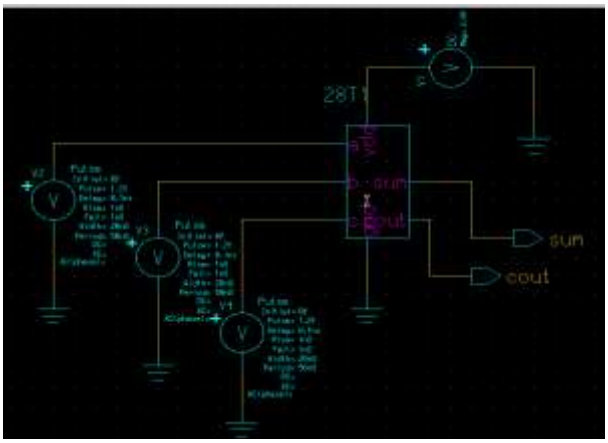

Figure 3: Test Circuit of Full Adder using 28 T

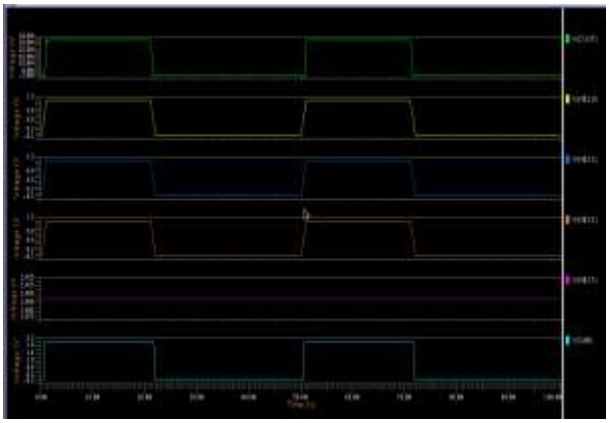

Figure 4: Full Adder Output Waveform of 28 T

1) Advantages

a. High noised margin.
b. Operates good even at low voltages.
c. Easily designed by use CMOS transistors.

2) Disadvantages

a. More power consumption.
b. Larger area.
c. More number of transistors lead to high input loads which gives low output.

3) Simulation Results For 28T Full Adder Schematic

Memory size allocated in Mbytes : 259.7
Latency : 0.000000%
Average number of newton iterations: 3.321101
No of components : 32
No of nodes : 74
No of MOS or BIP calls : 19442
Number of steps computed : 104
CPU TIME : 0s 080ms
GLOBAL ELAPSED TIME : 2s

B. 20 TRANSMISSION GATE FULL ADDER

Transistor count is reduced from the conventional type full adder. This design produces stored output for both SUM & CARRY. Instead of fixed power supply value, using pass transistor logic enables signal flow between drain & source.

It is different from CMOS logic in the view that source side of logic instead of using power lines, transits network & is connected to the input signal directly.

Circuit has 2 inverters & 2 transmission gates acting as 8 T XOR.

8 T XOR module is followed by.8T XNOR

Sum: C in and C in (bar) are multiplied, are controlled by (a XNOR) or (a XOR b)

Cout : a and c in are mul tiplied and controlled by [a (xor) b].

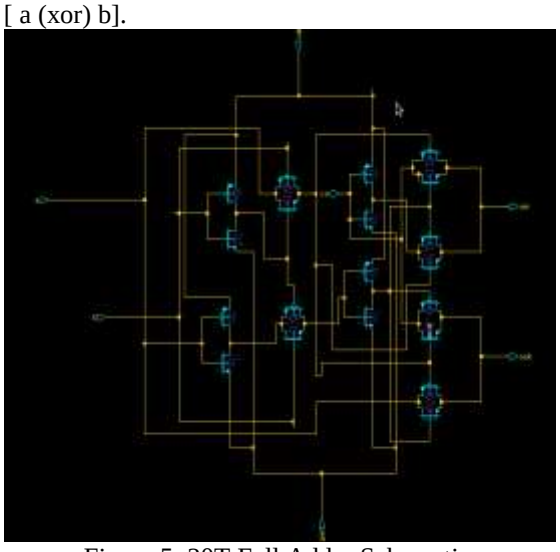

Figure 5: 20T Full Adder Schematic

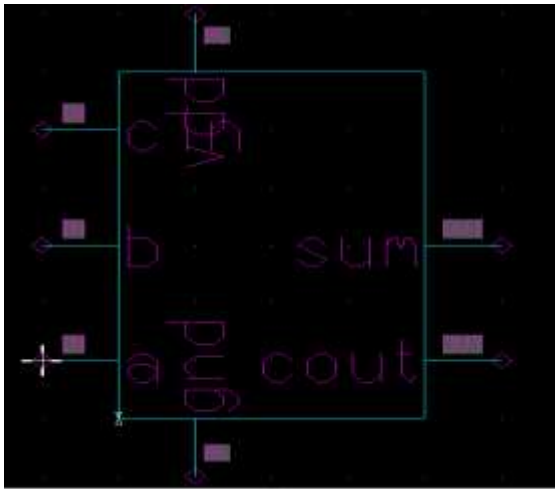

Figure 6 : 20T Full Adder Symbol

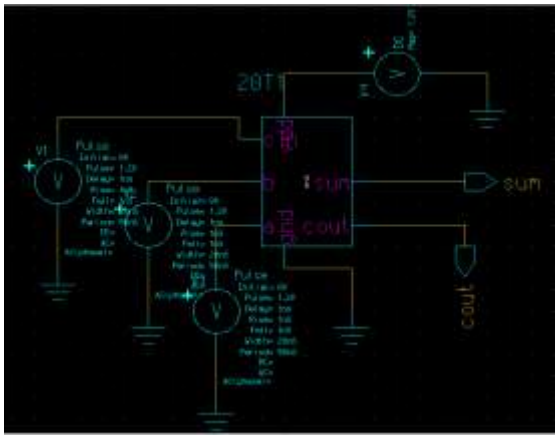

Figure 7: 20T Full Adder Test Circuit

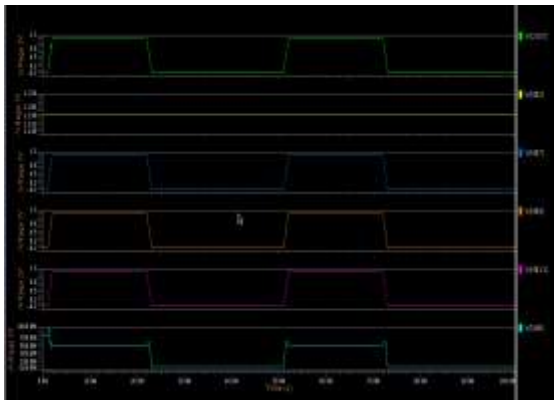

Figure 8: Output Waveform For 20T Full Adder Circuit

1) Advantages

a) *Simpler* than conventional Adder.
b) Faster than conventional Adder.
c) Smaller *input* loads to give large output.
d) Pass *transistors* used here required low power.
e) Reduced *complexity*.
f) Reduced *siliconarea*.

2) Disadvantages

a) More power dissipation than conventional Adder.
b) High power consumption.

3) Simulation Results For 20T Full Adder Schematic

Memory size allocated in Mbytes : 259.7
Latency :
0.000000%
Average number of newton iterations
:3.113636
No of components : 24
No of nodes :72
No of MOS or BIP calls :10637
Number of steps computed : 82

CPU TIME :0s
060ms
GLOBAL CPU TIME :0s
320ms
GLOBAL ELAPSED TIME :*2s*

V. OBSERVATION AND ANALYSIS

The following observations can be made based on the designs discussed.

Properties For Adder Schematic	
CELL NAME	**PROPERTIES**
PMOS	W = 2µ & L= 0.13 µ
NMOS	W =2 µ & L= 0.13 µ
V PULSE	V=1.2 V, td= 1ns Trise= Tfall=0.1ns T=20 ns
V DC	V dc =1.2 v

Table 2 : Properties For Adder Schematic

VDD(In volts)	**Power dissipated(In Watts)**	
ADDERS	**28T**	**20T**
1.2	4.87N	215.8U
1.4	6.39N	357.5U
1.6	8.20N	541.3U
1.8	10.4N	769.7U
2.0	12.9N	1.05M

Table 3: Performance Parameters

VI. CONCLUSIONS

The main objective is to improve the performance specifications of full ad der such as to reduce the overall power dissipated in the circuit with less number of transistors in order to reduce area. This circuit was designed with 0.13 µm technology. Due to less number of transistors and less power dissipation 20T adder is quite useful in portable applications.

VII. FUTURE SCOPE

All these adders can also be implemented using the BICMOS circuit techniques in the future to increase speed and to reduce power. BICMOS circuits are combination of bipolar transistors and CMOS transistors. They acquire the property of high speed from the bipolar transistors and the property of low power from CMOS transistors. Thus using BICMOS will result in more efficient adder designs.

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