Power Quality Analysis of Three Phase Voltage Source Inverter using various SVPWM switching schemes

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Abstract *— Voltage Source Inverters (VSI) are employed for variable voltage/ variable frequency adjustable speed drives. The Space Vector Pulse Width Modulation (SVPWM) scheme when applied to VSIs, it improves the effective dc bus utilization and lowers the Total Harmonic Distortion (THD). It also takes care of Electro Magnetic Interference (EMI) reduction, switching loss minimization and better spreading of harmonic spectrum. There are six different SVPWM schemes applied to VSIs are discussed in this paper and its THD spectrum for each scheme using Matlab/Simulink environment is depicted. The simulation results are validated with a prototype using Spartan 3E Field Programmable Gate Array (FPGA) board.*

Keywords *— Voltage Source Inverters (VSI), Space vector switching pattern, Total Harmonic Distortion (THD), Digital pulses.*

I. INTRODUCTION

In recent years, Space Vector Pulse Width Modulation (SVPWM) technology finds widespread applications in the filed of power electronics and electrical drives [1,2]. The dc utilization ratio in SVPWM scheme is very much increased, which is 70.7% of dc link voltage when compared to Sinusoidal Pulse Width Modulation (SPWM). The SVPWM scheme lowers the switching loss, maximizes the dc bus utilization and reduces the harmonic content in the output voltage.

The multi-sampled SVPWM scheme improves the performance of three phase VSIs. FGPGA based SVPWM pulse generation methodology is the mostly used digital platform for generating pulses for three phase VSI. It's become more popular because of its better performance, faster rate and low cost [3, 4]. The lower order harmonics of the output voltage in VSI very much reduced in FPGA based SVPWM platform.

The researchers have been striving hard to develop a new SVPWM strategy for Voltage Source Inverters [5-9]. This paper deals with six SVPWM schemes for three phase VSI shown in Fig.1. The simulation is carried out in Matlab/Simulink and output voltage FFT analysis is done to find the THD of the each scheme. The SVPWM pulses for the VSI are realised using Spartan 3E FPGA.

II. SVPWM GENERATION

The three phase quantities are represented in two dimensional vectors (α, β) plane for Space Vector Pulse Width Modulation (SVPWM) strategy based VSI. In space vector, output voltage of inverter is rotating in clockwise direction with notation V as shown in Fig.2

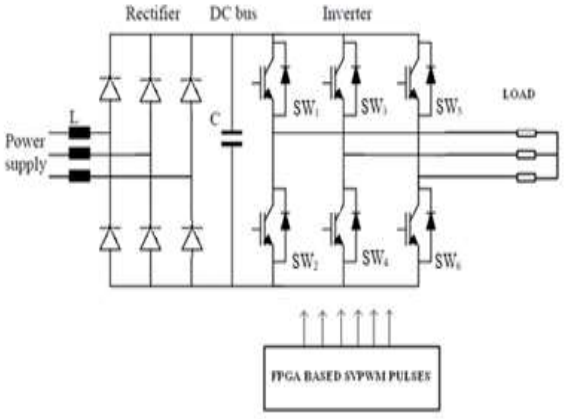

Fig.1. FGPA pulse switched 3ϕ VSI

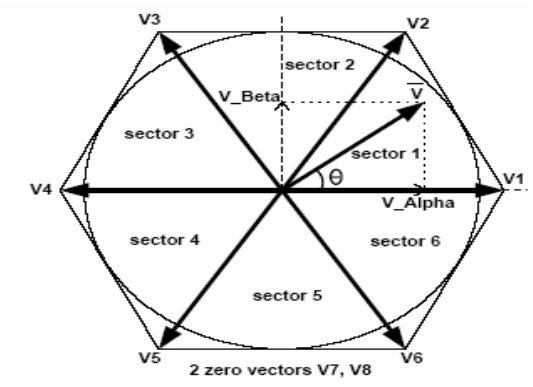

Fig.2. Sector Representation

The SVPWM generation is realized by determining two phase quantities and time duration of each transistor. The Clark's transformation has been applied in the stationary reference frame to find the magnitude and angle of rotating vector [9]

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

$$|V_{ref}| = \sqrt{{V_d}^2 + {V_q}^2}$$

$$t_1 = t_z\alpha\frac{\sin(\pi/3 - \alpha)}{\sin(\pi/3)}$$

$$t_2 = t_z\alpha\frac{\sin(\alpha)}{\sin(\pi/3)}$$

$$t_0 = t_Z - t_1 - t_1$$

Where

$0 \leq \alpha \leq 60$

t_Z = Switching Time

The six switching patterns are introduced and corresponding timing instants of upper switches for each sector is presented in Table 1 and Table 2. The symmetry nature and arrangement vector of first pattern helps to reduce the PWM switching timings. In the second pattern, null vector [0 0 0] has been fixed to for all the six sectors and number of switching per will be less. All the sectors of third pattern has been assigned with the null vector [1 1 1]. In the fourth pattern, the sequence of the non-zero voltage vectors remains unchanged within the sector. The sector 1,3,5 has been assigned with Null vector [1 1 1] and sector 2,4,6 has been with null vector [0 0 0]. The null vectors in the fourth pattern are interchanged for the sectors as in that case of fifth pattern in the sense null vector [1 1 1] is fixed for the sector 2,4 and 6 and [0 0 0] is fixed for 1,3 and 5. In sixth pattern, null vector is not used for any of the six sectors.

Table I SWITCHING TIMING INSTANT FOR EACH SECTOR OF UPPER SWITCHES (PATTERN I, II AND II)

Sector	Pattern I	Pattern II	Pattern III
1	$Sw_1=t_1+t_2+t_0/2$ $Sw_2=t_2+t_0/2$ $Sw_3=t_0/2$	$Sw_1=t_1+t_2$ $Sw_2=t_2$ $Sw_3=0$	$Sw_1=t_1+t_2+t_0$ $Sw_2=t_2+t_0$ $Sw_3=t_0$
2	$Sw_1=t_1+t_0/2$ $Sw_2=t_1+t_2+t_0/2$ $Sw_3=t_0/2$	$Sw_1=t_1$ $Sw_2=t_1+t_2$ $Sw_3=0$	$Sw_1=t_1+t_0$ $Sw_2=t_1+t_2+t_0$ $Sw_3=t_0$
3	$Sw_1=t_0/2$ $Sw_2=t_1+t_2+t_0/2$ $Sw_3=t_2+t_0/2$	$Sw_1=0$ $Sw_2=t_1+t_2$ $Sw_3=t_2$	$Sw_1=t_0$ $Sw_2=t_1+t_2+t_0$ $Sw_3=t_2+t_0$
4	$Sw_1=t_0/2$ $Sw_2=t_1+t_0/2$ $Sw_3=t_1+t_2+t_0/2$	$Sw_1=0$ $Sw_2=t_1$ $Sw_3=t_1+t_2$	$Sw_1=t_0$ $Sw_2=t_1+t_0$ $Sw_3=t_1+t_2+t_0$
5	$Sw_1=t_2+t_0/2$ $Sw_2=t_0/2$ $Sw_3=t_1+t_2+t_0/2$	$Sw_1=t_2$ $Sw_2=0$ $Sw_3=t_1+t_2$	$Sw_1=t_2+t_0$ $Sw_2=t_0$ $Sw_3=t_1+t_2+t_0$
6	$Sw_1=t_1+t_2+t_0/2$ $Sw_2=t_0/2$ $Sw_3=t_1+t_0/2$	$Sw_1=t_1+t_2$ $Sw_2=0$ $Sw_3=t_1$	$Sw_1=t_1+t_2+t_0$ $Sw_2=t_0$ $Sw_3=t_1+t_0$

Table II SWITCHING TIMING INSTANT FOR EACH SECTOR OF UPPER SWITCHES (PATTERN III AND IV)

Sector	Pattern IV	Pattern V	Pattern VI
1	$Sw_1=t_1+t_2+t_0/2$ $Sw_2=t_2+t_0$ $Sw_3=t_0$	$Sw_1=t_1+t_2$ $Sw_2=t_2$ $Sw_3=0$	$Sw_1=t_1+t_2$ $Sw_2=0$ $Sw_3=t_1$
2	$Sw_1=t_1$ $Sw_2=t_1+t_2$ $Sw_3=0$	$Sw_1=t_1+t_0$ $Sw_2=t_1+t_2+t_0$ $Sw_3=t_0$	$Sw_1=t_1+t_0$ $Sw_2=t_2$ $Sw_3=t_0$
3	$Sw_1=t_0$ $Sw_2=t_1+t_2+t_0$ $Sw_3=t_2+t_0$	$Sw_1=0$ $Sw_2=t_1+t_2$ $Sw_3=t_2$	$Sw_1=t_1$ $Sw_2=t_1+t_2$ $Sw_3=0$
4	$Sw_1=0$ $Sw_2=t_1$ $Sw_3=t_1+t_2$	$Sw_1=t_2$ $Sw_2=t_1+t_0$ $Sw_3=t_1+t_2+t_0$	$Sw_1=0$ $Sw_2=t_1+t_2$ $Sw_3=t_2$
5	$Sw_1=t_2+t_0$ $Sw_2=t_1$ $Sw_3=t_1+t_2+t_0$	$Sw_1=t_2$ $Sw_2=0$ $Sw_3=t_1+t_2$	$Sw_1=0$ $Sw_2=t_1$ $Sw_3=t_1+t_2$
6	$Sw_1=t_1+t_2$ $Sw_2=0$ $Sw_3=t_1$	$Sw_1=t_1+t_2+t_0$ $Sw_2=t_0$ $Sw_3=t_1+t_0$	$Sw_1=t_2$ $Sw_2=0$ $Sw_3=t_1+t_0$

III. SIMULATION RESULTS

The three phase VSI using six SVPWM patterns is simulated for a switching frequency of 1 KHz to attain an output voltage of 200V with a balanced resistive load. The Matlab simulation model includes the sector calculation, timing calculation, switching sequence, control signals and inverter. The output voltage of SVPWM modulation using the first pattern is shown in Fig.3 The variations in the output voltage harmonic spectra for the all six patterns is depicted in Fig.4 to Fig.9. It is observed that the first pattern of output voltage contains lower harmonic content and higher fundamental voltage.

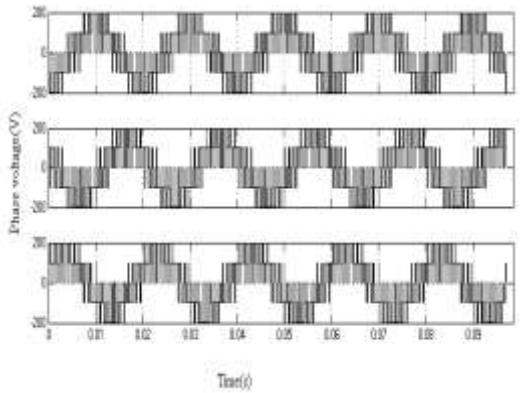

Fig.3. Phase Votlage Waveform for Pattern I

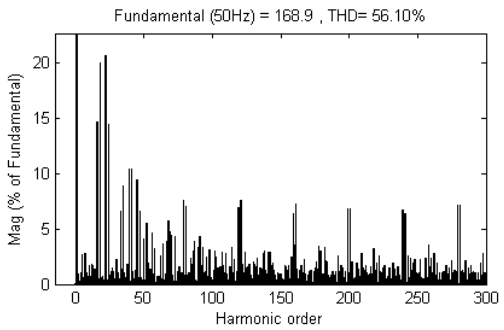

Fig.4. Phase Votlage spectrum for Pattern I

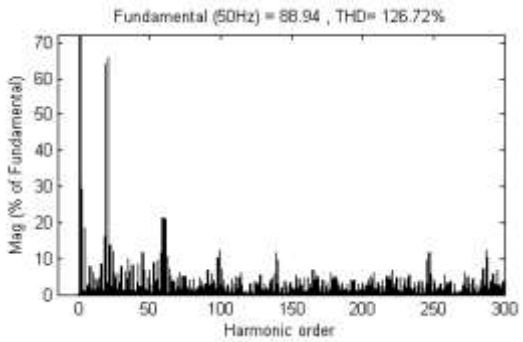

Fig.5. Phase Votlage spectrum for Pattern II

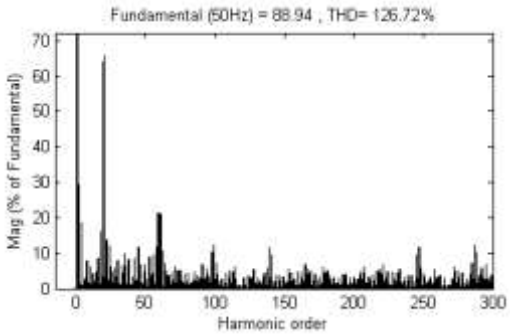

Fig.6. Phase Votlage Waveform for Pattern III

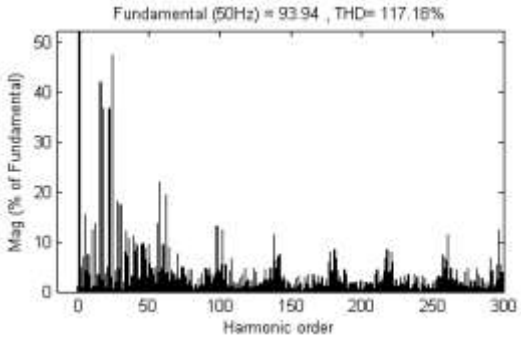

Fig.7. Phase Votlage Waveform for Pattern IV

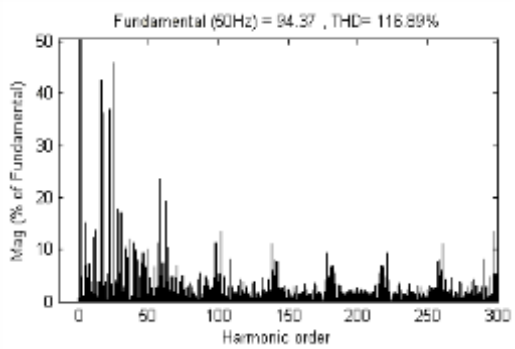

Fig.8. Phase Votlage Waveform for Pattern V

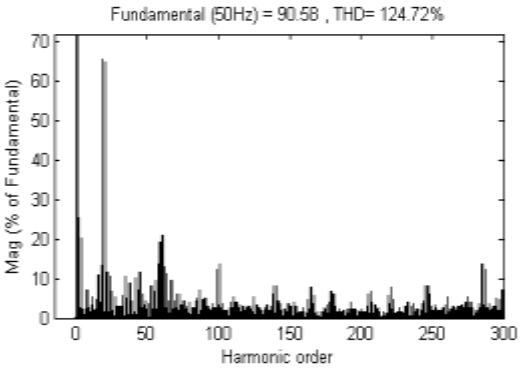

Fig.9. Phase Votlage Waveform for Pattern VI

IV. EXPERIMENTAL RESULTS

The SVPWM pulses generated using the FPGA based system generator is applied to a prototype model of a three phase inverter. The phase voltage waveform and its spectrum for all six patterns are captured through Tektronix TPS 2024 storage oscilloscope depicted in Fig. 10 to Fig.21. The experimental results authenticate the simulation results and thus validating the different SVPWM patterns for the three phase VSI.

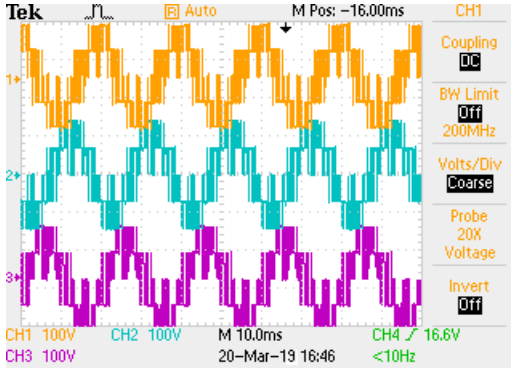

Fig.10. Phase Votlage waveform for Pattern I

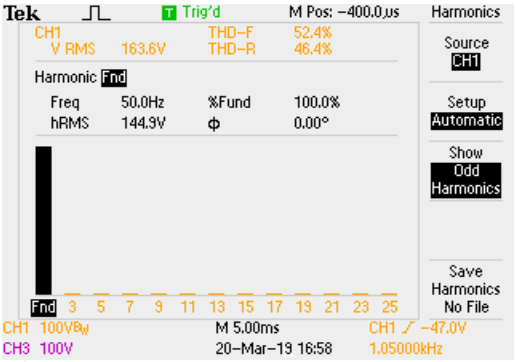

Fig.11. Phase Votlage spectrum for Pattern I

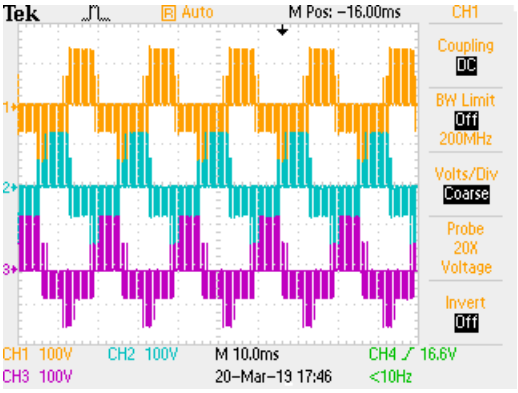

Fig.12. Phase Votlage waveform for Pattern II

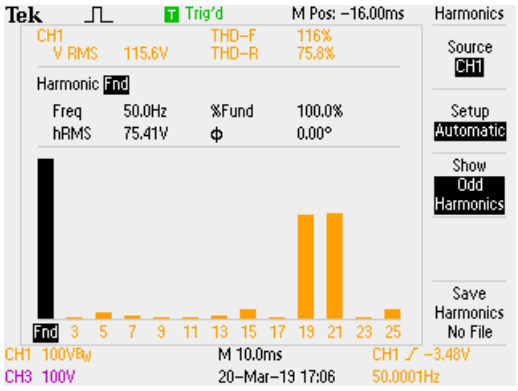

Fig.13. Phase Votlage spectrum for Pattern II

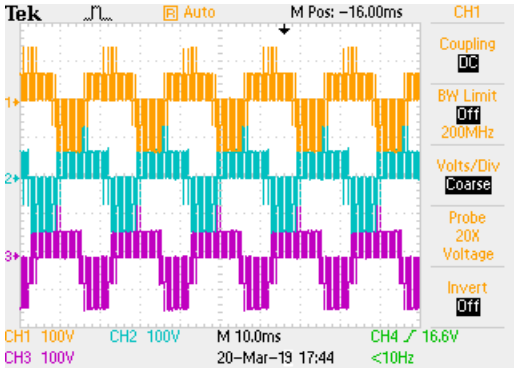

Fig.14. Phase Votlage waveform for Pattern III

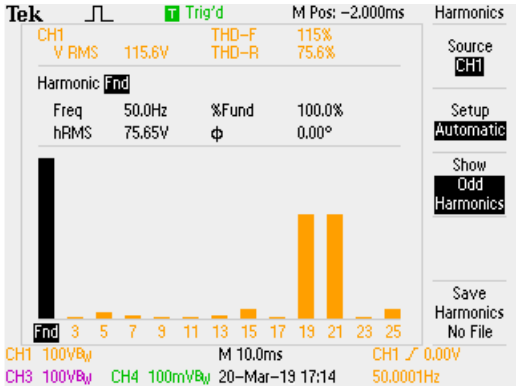

Fig.15. Phase Votlage spectrum for Pattern III

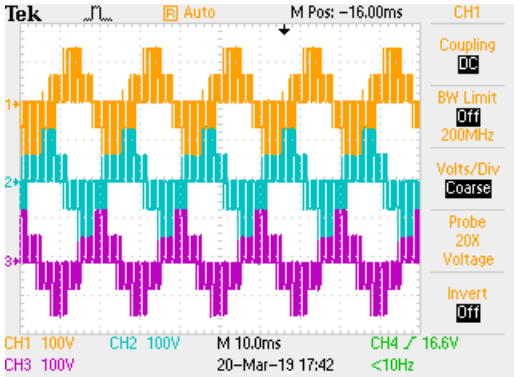

Fig.16. Phase Votlage waveform for Pattern IV

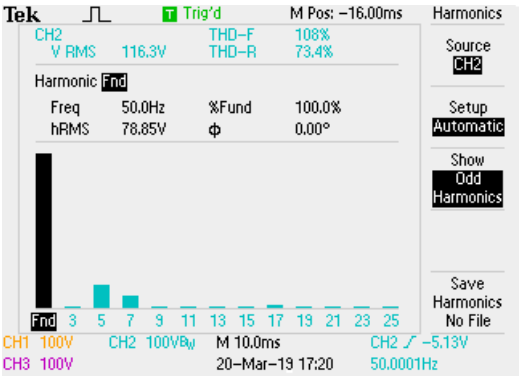

Fig.17. Phase Votlage spectrum for Pattern IV

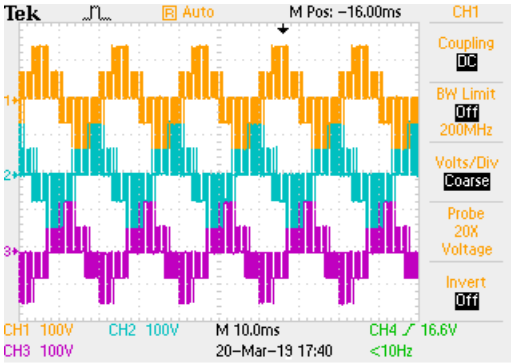

Fig.18. Phase Votlage waveform for Pattern V

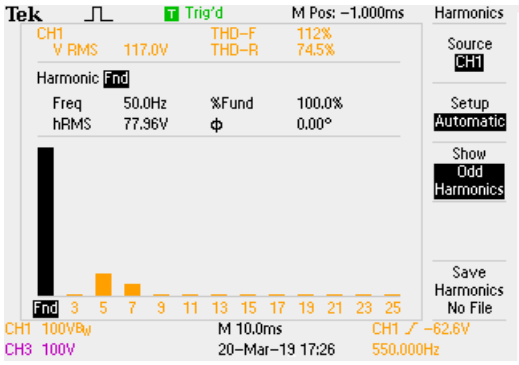

Fig.19. Phase Votlage spectrum for Pattern V

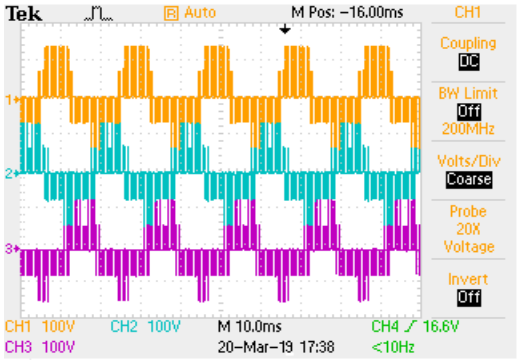

Fig.20. Phase Votlage waveform for Pattern VI

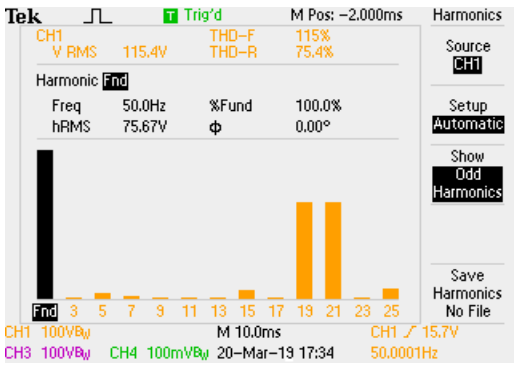

Fig.21. Phase Votlage spectrum for Pattern V

V. CONCLUSION

A model of space vector modulated three phase inverter is developed using MATLAB/ Simulink software. To facilitate the digital implementation of SVPWM scheme for three-phase inverter application, a compact algorithm using FPGA has been developed to generate different patterns. It is observed from the result that first scheme of SVPWM utilizes more dc link voltage and acquire less harmonic content.

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